TELEDYNE PHILBRICK

4129QZ 12-BIT ECONOMY A/D CONVERTER

Teledyne Philbrick Model 4129QZ is a low-cost, general purpose, 12-bit analog-to-digital converter that employs the successive approximation technique. The unit features an internal low-drift reference, an optional high-impedance input buffer, buffered 10 load TTL/DTL drive capability, and a maximum conversion time of 24 μsec. In addition, the unit can be externally programmed for input voltages of 0 to +10 V, 0 to +5 V, ±5 V or ±10 V.

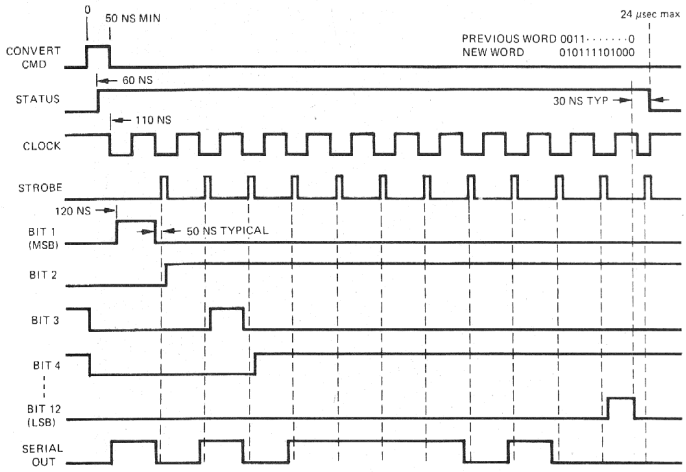
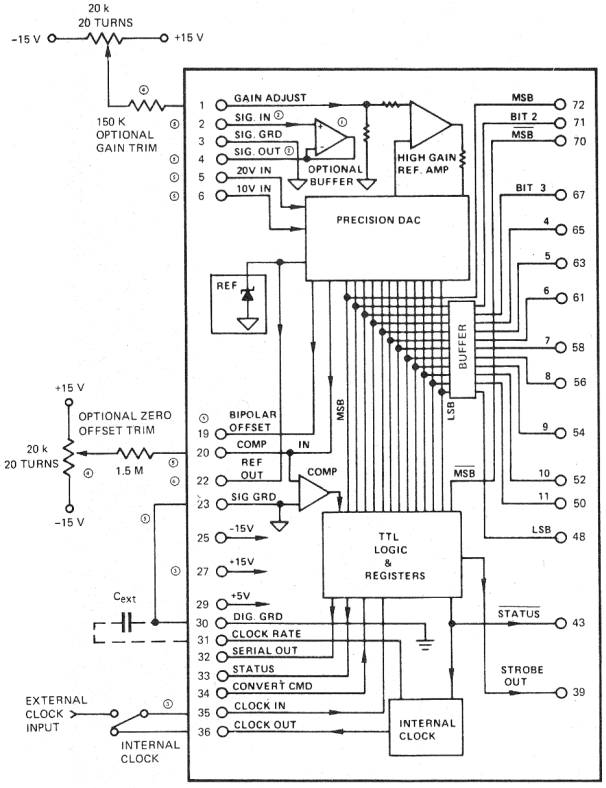


Figure 1. Timing Diagram



① OPTIONAL BUFFER AVAILABLE ON BUFFERED VERSION ONLY, MODEL 4129-10QZ
② PINS 2 AND 4 ARE INTERNALLY CONNECTED ONLY ON MODEL 4129-10QZ.
③ SIGNAL GROUND AND DIGITAL GROUND MUST BE EXTERNALLY CONNECTED. FOR NORMAL OPERATION CLOCK OUT AND CLOCK IN MUST BE EXTERNALLY CONNECTED.
④ USE CERMET POTENTIOMETERS AND METAL FILM RESISTORS. IF GAIN AND OFFSET TRIM IS NOT REQUIRED LEAVE PINS 1 AND 20 OPEN.
⑤ SEE PIN PROGRAMMING TABLE FOR PROPER INPUT CONNECTIONS.
⑥ REFERENCE VOLTAGE SHOULD BE OBTAINED THROUGH HIGH INPUT IMPEDANCE BUFFER.

Figure 2. Functional Block Diagram

FEATURES

- 12-Bit Resolution
- Fully Buffered Parallel and Serial Outputs
- 24 μsec Conversion Time, max

APPLICATIONS

- Data Acquisition Systems
- Test & Measuring Equipment
- General Purpose

MODEL	INPUT IMPEDANCE	CONVERSION TIME
4129QZ	2.5 kΩ (5V Input) 5 kΩ (10V Input) 10 kΩ (20V Input)	24 μsec Max.
4129-10QZ	10^{10} Ω (5, 10, 20V)	24 μsec Max.

Table 1. Tabulation of Models

TRIM PROCEDURES

Zero Offset Trim Procedure – Set input voltage to precisely 1/2 LSB unipolar, or –F.S. + 1/2 LSB bipolar. Adjust zero offset trim potentiometer (See Figure 2) until the converter is on the threshold of switching from 000...000 to 000...001.

Gain Trim Procedure – Set input voltage to precisely F.S. –1 1/2 LSB. Adjust gain trim potentiometer (See Figure 2) until the converter is on the threshold of switching from 111...110 to 111...111.

INCREASING CONVERSION TIME

The Conversion Time can be increased by adding external capacitance from Clock Rate to Digital Ground. The new Conversion Time, t , is determined from the following equation:

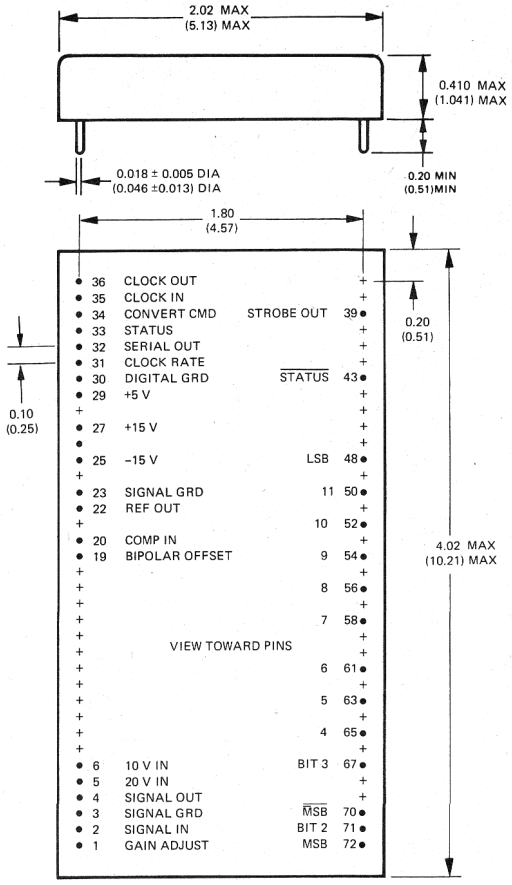
$$t \cong 23\ \mu\text{sec}\ (1 + \frac{C_{ext}}{4700\text{pF}})$$

where conversion time is measured in microseconds and C_{ext} is expressed in pF.

SPECIFICATIONS (At 25°C, ±15V, unless otherwise indicated)

	TYPICAL	GUARANTEED
RESOLUTION	---	12 Bits
INPUTS		
Analog		
Voltage Ranges	±5 V, ±10 V, 0 to +5 V, 0 to +10 V	
Impedance, Direct (4129 QZ) ±1%	2.5 KΩ (5 volt) 5 KΩ (10 Volt) 10 KΩ (20 Volt)	
Impedance, Buffered (4129-10 QZ)	---	10^{10} Ω
Power	+15 V ±5% at 50 mA max.	
	−15 V ±5% at 60 mA max.	
	+5 V ±5% at 200 mA max.	
Recommended Philbrick Supply	2242 or 2243	
Digital		
Convert Command		
Logic	TTL Positive Pulse; DC coupled	
Conversion Initiation	---	0 to 1 state
Pulse Width, min./max.	---	0.05/20 μsec
Loading	---	1 TTL Load
Clock In		
Logic	TTL negative pulse	
Loading	---	2 TTL Loads
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity	---	± ½ LSB
Differential Nonlinearity	±¼ LSB	± ½ LSB
Quantization Error	---	± ½ LSB
Monotonicity		+13 to +37 °C
Zero Offset Error, Unipolar ⑤	---	±20 mV
Zero Offset Error, Bipolar ⑤	---	±5 LSB
Gain Error ⑤	---	±0.2%
Stability		
Differential Nonlinearity vs. Temp. ①	±4 ppm of Range/°C	±10 ppm of Range/°C
Zero Offset Error vs. Temp., Unipolar ①	---	±5 ppm of Range/°C
Zero Offset Error vs. Temp., Bipolar ①	---	±10 ppm of Range/°C
Gain Error vs. Temp. ①	---	±30 ppm of Reading/°C
Zero Offset Power Supply Sensitivity ②	---	±10 ppm/%△V_{cc}
Gain Power Supply Sensitivity ②	---	±20 ppm/% △ V_{cc}
Dynamic Characteristics		
Conversion Time ③ ④	---	24 μsec
OUTPUTS		
Analog Reference		
Voltage	---	+6.2 V ± 5%
Current	---	1 mA
Digital		
Logic Codes, Parallel, Unipolar	Binary	
Logic Codes, Parallel, Bipolar	Offset Binary or 2's Complement	
Output Drive (MSB and $\overline{\text{MSB}}$)	---	6 TTL Loads
Output Drive (all other bits)	---	10 TTL Loads fully buffered
Logic Codes, Serial, Unipolar	Binary	
Logic Codes, Serial, Bipolar	Offset Binary	
Format	NRZ	
Output Drive	---	10 TTL Loads fully buffered
Switching Levels, all digital outputs ⑥		
"0" State	---	⩽ +0.4 V
"1" State	---	⩾ +2.4 V
Status		
"0" State	Before and After Conversion	
"1" State	During Conversion	
Output Drive	---	5 TTL Loads
$\overline{\text{Status}}$		
"0" State	During Conversion	
"1" State	Before and After Conversion	
Output Drive	---	10 TTL Loads
Strobe Output		
Logic	---	TTL Positive Pulse
Output Drive	---	10 TTL Loads
Clock Output		
Logic	TTL Negative Pulse	
Output Drive	---	4 TTL Loads
ENVIRONMENTAL CHARACTERISTICS		
Operating Temperature Range	---	0 to +70 °C
Storage Temperature Range	---	−55 to +125 °C
Relative Humidity	95% non-condensing	---
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage to Ground, ±15 V/+5 V	---	±18 V/+7 V
Digital Input Voltage	---	5.5 V
Analog Input Voltage, 4129 QZ	---	±25 V
4129-10 QZ	---	±V_{cc}
Short Circuit Protection, all digital outputs ⑦		
To Ground	---	1 second

① Range for unipolar operation ≡ +F.S.; Range for bipolar operation ≡ 2 (+F.S.).
Reading for bipolar input is defined as |Actual Reading −(−F.S.)|.
② For ±15 V supply only, no observable change with +5V variation in +% V supply
③ Conversion time is measured from trailing edge of convert command pulse to "1" −"0" transition of status output.
④ Faster units available. Consult Factory.
⑤ Adjustable to zero
⑥ One TTL Load is identical to that defined for standard 54/74 Series TTL.
⑦ Except for MSB, $\overline{\text{MSB}}$ and Status, which are not protected for short circuit to ground.



±0.01 Non-cumulative tolerance between pins
±0.02 Tolerance from case edge to center of pins

DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS

Optional Socket: Model 6135

Figure 3. Mechanical Configuration

Input Range in Volts	Input	Range and Buffer Select: Input to pin	Range and Buffer Select: Jumper pin 4 to	Range and Buffer Select: Jumper pin 20 to	Offset Select Jumper pin 19 to
0 to +10 V	Unbuffered	6	–	–	23
	Buffered*	2	6	–	23
±5 V	Unbuffered	6	–	–	20
	Buffered*	2	6	–	20
±10 V	Unbuffered	5	–	–	20
	Buffered*	2	5	–	20
0 to +5 V	Unbuffered	6	–	5	23
	Buffered*	2	6	5	23

*Buffered input can be used only with 4129-10QZ.

Table 2. Range Setting

POWER AND GROUNDING CONSIDERATIONS

Models 4129QZ and 4129-10QZ are provided with internal 1 μF tantalum, and 0.01 μF disc, power supply bypass capacitors. In addition, it is important to remember that Signal Ground and Digital Ground must be externally connected to ensure that there are no ground loop errors.

TELEDYNE PHILBRICK