Applications Bulletin

TELEDYNE PHILBRICK

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APPLICATIONS FOR THE MODEL 4110 TRACKING ANALOG TO DIGITAL CONVERTER

Multi-Channel Simultaneous Sample-Hold Systems

The data acquisition system illustrated in Figure 1. can replace the conventional analog multiplexer approach. The advantage of this multi-channel simultaneous sample-hold system is a far superior cost/performance ratio compared to a multiple sample-hold, analog multiplexed, high speed successive approximation A/D converter system.

In this application all 4110's independently track their respective inputs on a real time basis. Data can be read or stored by simply grounding the Inhibit line to "freeze" all data outputs simultaneously.

Systems of this type are used in acoustical analyzers and seismic work including oil exploration, earthquake location instrumentation, and nuclear explosion detection and location.

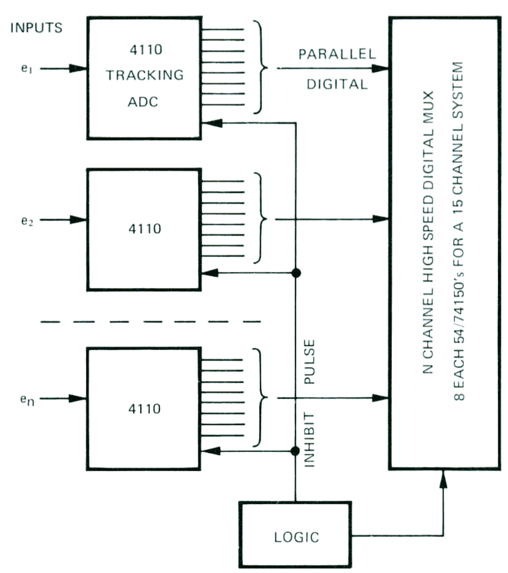


Figure 1.

Long Term, Low Drift Analog Multiplier

Analog multiplication can be performed with a 4110 and a multiplying DAC such as Philbrick's 4028 (see Figure 2). The advantages of this technique are excellent accuracy at high and low signal levels, and low drift with time and temperature.

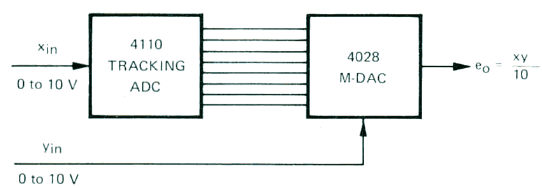


Figure 2.

Function Generation at 10 kHz

A precision analog function of an independent variable (such as cos x, log x, $\sqrt{x}$) is conventionally developed in analog fashion using loggers, square-rooters, etc. But one can also do it digitally by addressing a read-only-memory (ROM) with the output of a 4110 ADC (see Figure 3). The contents of the ROM (table of sines, cosines, or some arbitrary function) is then fed to a DAC, such as the Philbrick 4021, to provide the analog signal.

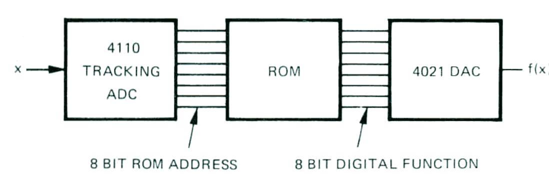


Figure 3.

The 4110: A Time Machine

It is often necessary to expand or contract time relative to the acquisition, display, and/or storage of analog data. This usually requires magnetic tape recording, film recording, strip charts, etc. — all expensive and bulky. By the use of analog conversion and digital memory technology, however, these functions can be performed quite simply by placing a memory between a tracking ADC and a DAC. See Figure 4.

Time Expansion

Suppose it is desired to record a 25 μsec piece of transitory analog information on a one Hz chart recorder: (See Figure 4.) The 25 μsec analog signal is digitized by the 4110. The timing circuits clock the 8-bit parallel data into Fairchild 4130 Memories at a 2 MHz word rate, freezing the 4110 output for each word to insure clean unchanging data. The 4130 is a 64-bit FIFO (First In-First Out) device. Thus, in 25 microseconds it will be given 50 words from the 4110. At the end of the 25 μsec period the Timing Circuits will clock the data from Memory into the DAC at a rate suitable for recording — say about 1 word per second at a paper speed of 0.1 inch per second.

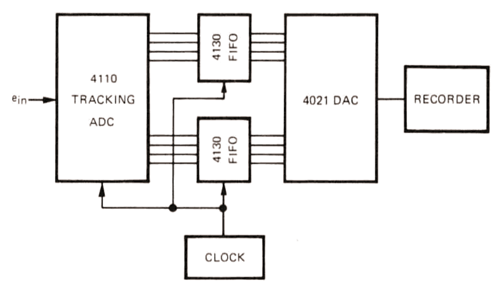


Figure 4.

Time Contraction

The same functional circuit may be used to speed up time for the display of slow phenomena on a standard oscilloscope (rather than a long persistence scope, a storage scope or a magnetic tape loop). For example, during a slow chemical reaction lasting several minutes or hours, temperature, pressure, flow, etc. may be digitized with a Model 4110 per parameter, and each stored in its own memory. If asynchronous data is desired, each point stored may be initiated by significant events or values of one or more of the variables rather than from a clock.

At the completion of the reaction the memory may be clocked out very rapidly into a multi-channel standard oscilloscope. If displayed in this way, however, the data will be displayed only once, leaving little time for evaluation unless photographed. By the addition of a feedback loop from Memory Out to Memory In during the playback mode the phenomena can be displayed continuously, as it will be continuously clocked into and out of memory. If it is desired to record the data on a strip chart after cursory analysis, it may be clocked out of memory at a rate compatible with available recorders. If more than 64 words of memory are desired, it may be expanded to n words in 64-bit groups.

Non-Frequency Dependent Analog Time Delay

Analog time delay can be performed using the same combination of devices as the digital delay shown in Figure 4. In this application data is clocked in and out of the FIFO memory at the same rate. If a 1 MHz clock is used the memory will provide 64 μsec of delay. If a 1 Hz clock is used 64 seconds of delay can be provided. Since the memories can be connected in series, additional delay is easily added.

Applications for such a circuit are numerous, but here are a couple of interesting ones:

1. Delay Analog Input Data.
   Analog data may require a delay so that a digital computer can analyze what is to be done with it. For example, the computer may scale the amplitude of the analog input with a multiplying DAC. This is essentially a precision AGC circuit in which no information is lost. See Figure 4a.

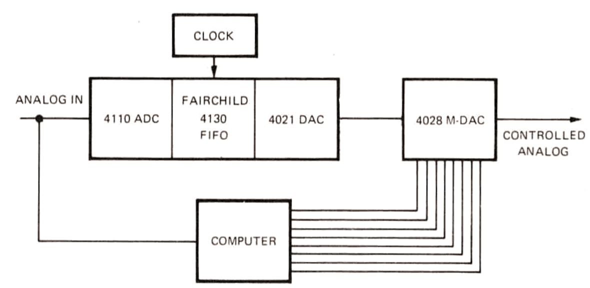


Figure 4a.

2. Audio Signal Time Delay
   The time delay can be varied simply by changing the clock rate. With a 640 element memory (similar to the one shown) the delay time will always be 640 times greater than the clock period. See Figure 4b.

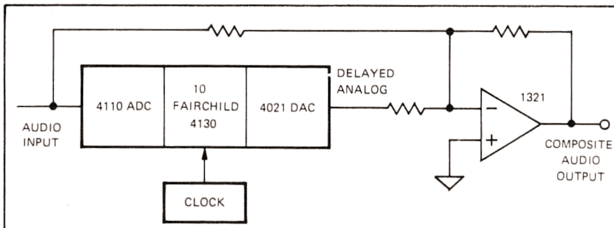


Figure 4b.

Peak Detector & Hold or Infinite Time Pulse Stretcher

The maximum value of a parameter during a process or test can be easily determined using the 4110 tracking ADC. An example of this application is measuring the maximum pressure from a pressure gage during an explosion, or determining the maximum stress indication from a strain gage during a destructive stress test. (See Figure 5.)

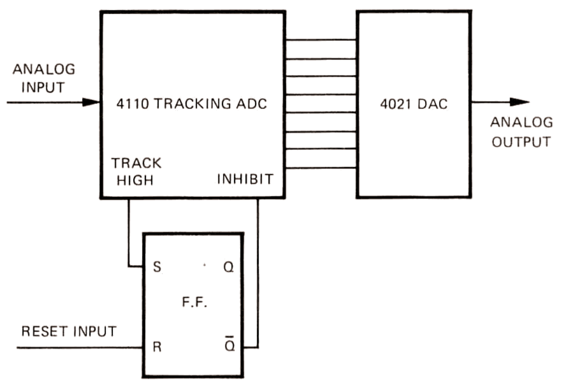
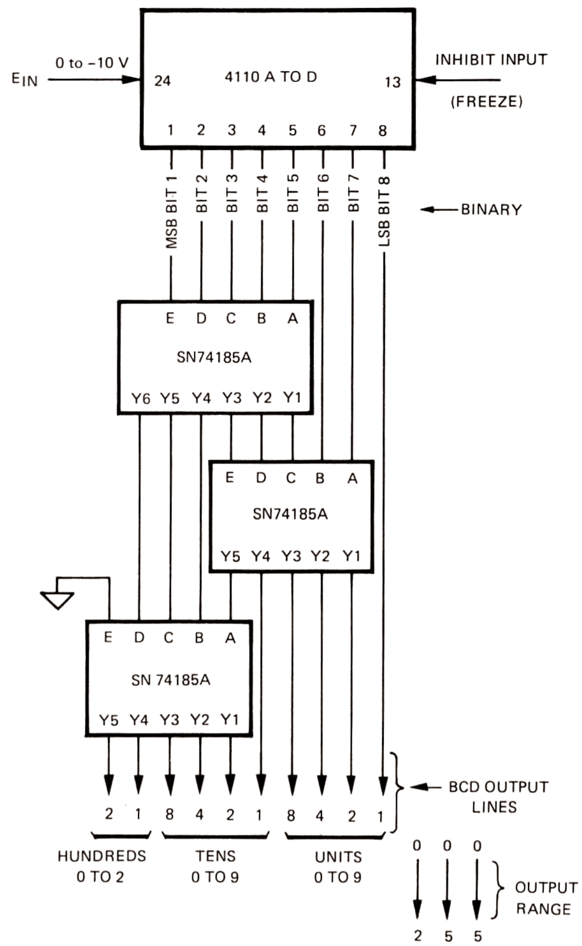


Figure 5. Positive Peak Detector*

* USE THE "TRACK LOW" OUTPUT FOR A NEGATIVE PEAK DETECTOR

The Model 4110's TRACK HIGH and TRACK LOW outputs are the key to this circuit. The 4110 is an inverting ADC, i.e., as the input goes negative the digital output is increasing toward all "ones." When the input goes positive, therefore, we get a TRACK LOW pulse for every count pulse. The instant the input signal starts to turn around, a TRACK HIGH pulse appears and inhibits any further change. To repeat the operation, hold the flip flop in reset for approximately 30 μsec.

FOR BINARY CODED DECIMAL APPLICATIONS



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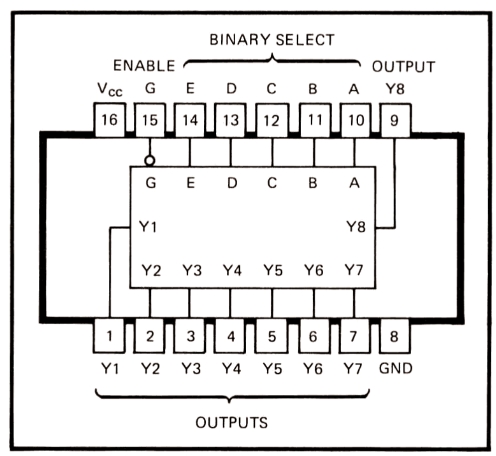

BCD OUTPUT FROM TELEDYNE PHILBRICK 4110 "TRACKING" A TO D CONVERTER

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