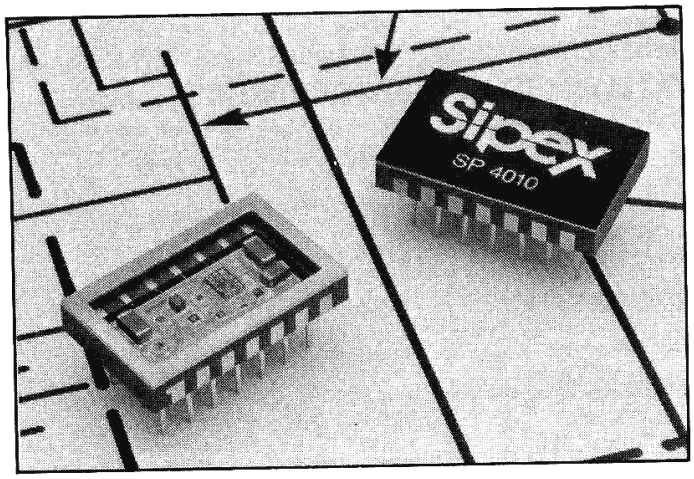
WIDE BANDWIDTH, HIGH ACCURACY, HIGH SPEED BUFFER

FEATURES

- Bandwidth: 60 MHz
- High slew rate: 1000V/μsec min
- Low offset and drift: 1mV/10μV/°C
- FET input
- 16-bit linearity @ ± 10VDC; 1kΩ load
- Voltage gain of 1 ±0.002%
- Settling time: 100nsec to 0.005% (5V step)
  200nsec to 0.005% (20V step)

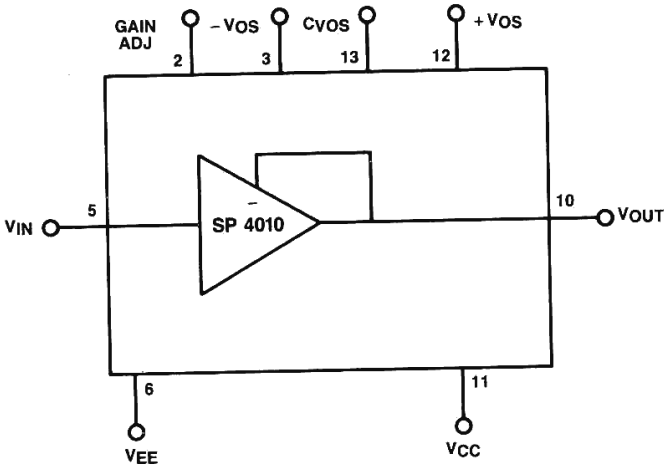


DESCRIPTION

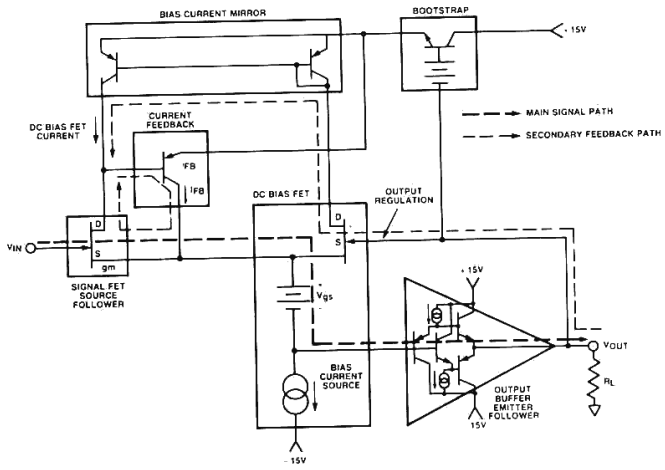
The SP4010 is a high accuracy, high speed, FET input buffer providing up to ±50 mA of continuous current at frequencies from DC to 60 MHz. High linearity, low offset, and excellent stability make it an ideal candidate for a high impedance input buffer for high resolution A/D converters. With a slew rate of 1000V/μsec, good phase linearity and low distortion, the SP4010 is also well suited for a variety of video and high speed data acquisition applications.

The SP4010 is specified for operation from 0°C to +70°C for commercial grade and −55°C to +125°C for military grades.

FUNCTIONAL DIAGRAM



SIMPLIFIED SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

MODEL	SP 4010C	SP 4010B
Supply Voltage	±18V	±18V
Input Voltage	V_{SUPPLY}	V_{SUPPLY}
Power Dissipation	1 Watt	1 Watt
Continuous Output Current	50mA	50mA
Peak Output Current	100mA	100mA
Operating Temperature Range	0°C to +70°C	−55°C to +125°C
Operating Junction Temperature	150°C	150°C
Case to Junction Thermal Resistance	20°C/Watt	20°C/Watt
Storage Temperature	−65°C to +125°C	−65°C to +150°C

DC ELECTRICAL CHARACTERISTICS

(Typical @ +25C, V_{CC} = +15VDC, VEE = −15 VDC unless otherwise specified)

MODEL	SP 4010C	SP 4010B
Input Bias Current[1]	100pA	100pA
Input Impedance	1GΩ	1GΩ
Input Capacitance	5pF	5pF
Output Offset Voltage[2]	±1mV typ, ±2mV max	±1mV typ, ±2mV max
Offset Voltage T_C	±10μV/°C	±10μV/°C typ ±50μV/°C max
Output Impedance	±0.1Ω	±0.1Ω typ, ±0.5Ω max
Output Voltage Swing (1kΩ Load)	V_{CC} −4.5V to V_{EE} +4V	V_{CC} −4.5V to V_{EE} +4V
Output Current	±25mA @ V_{OUT} = ±10V	±25mA@ V_{OUT}= ±10V ±50mA @ V_{OUT} = ±5V
Supply Current (Quiescent)	10mA	10mA typ, 14mA max
Power Consumption (Quiescent)	300mW	300mW
PSRR	0.001%/%	0.001%/%
Gain (1K Load)[2]	1±0.002% typ, ±0.02% max	1±0.002% typ, ±0.02% max
±10V Linearity Error (>1K Load)	±0.0005% typ. ±0.002% max	0.0005% typ. ±0.002% max

AC ELECTRICAL CHARACTERISTICS

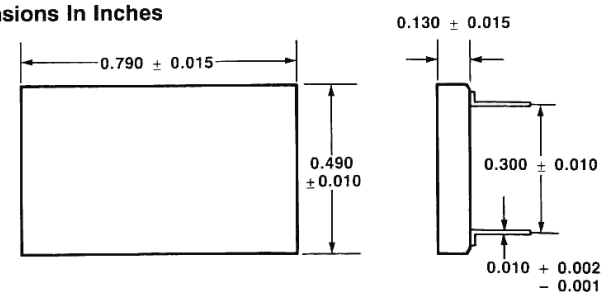
(Typical @ +25 C, V_{CC} = +15VDC, V_{EE} = 15VDC unless otherwise specified)

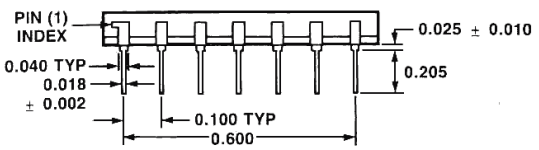
MODEL	SP 4010C	SP 4010B
Slew Rate	±1000V/μsec	±1000V/μsec min
Bandwidth	60 MHz	60 MHz
Harmonic Distortion Ω		
@10 kHz ($20V_{p-p}$, 1KΩLoad)	−100dB typ, −90dB max	−100dB typ, −90dB max
@1 MHz ($10V_{p-p}$, 1KΩLoad)	−80dB	−80dB
@10 MHz ($5V_{p-p}$, 1KΩLoad)	−60dB	−60dB
Settling Time (to 0.005%, ±20V Step) 1KΩLoad	200nS typ, 300nS max	200nS typ, 300nS max
Settling Time (to 0.005%, ±5V Step) 1KΩ Load	100nS typ, 200nS max	100nS typ, 200nS max
Noise Voltage Density	20nV/Hz	20nV/Hz

NOTES
1. Independent of input voltage if allowable swing is not exceeded.
2. Adjustable to zero. See gain/offset adjust procedure.

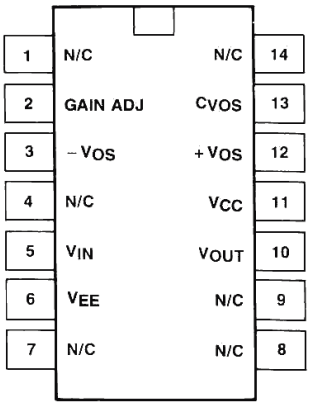
PACKAGE OUTLINE

Dimensions In Inches





PIN ASSIGNMENTS



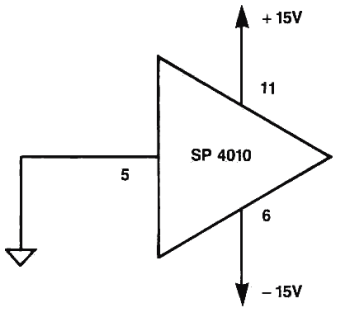
TOP VIEW

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	N/C	14	N/C
2	GAIN ADJ	13	C_{VOS}
3	$-V_{OS}$	12	$+V_{OS}$
4	N/C	11	V_{CC}
5	V_{IN}	10	V_{OUT}
6	V_{EE}	9	N/C
7	N/C	8	N/C

INTERNAL ACTIVE DEVICE	COUNT
Bipolar Transistors	41
JFET	2
DIODES	5

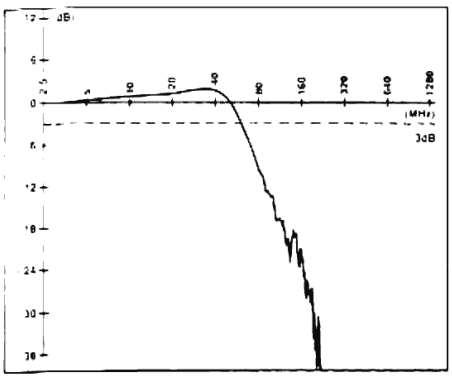
BURN IN SCHEMATIC



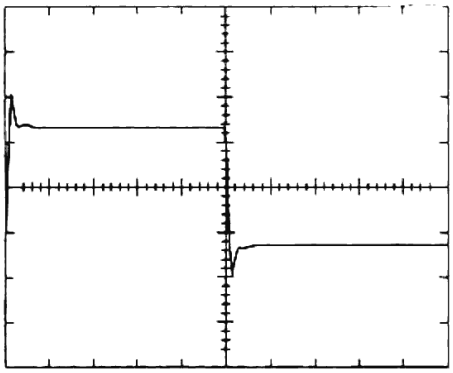
ORDERING INFORMATION

MODEL	TEMP RANGE	SCREENING
SP 4010B	−55°C to +125°C	MIL-STD-883C
SP 4010C	0°C to 70°C	—

TYPICAL PERFORMANCE CHARACTERISTICS

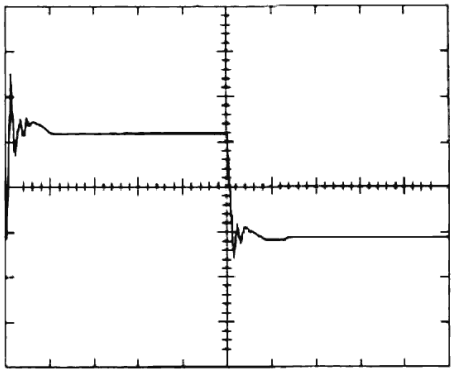


Small Signal Bandwidth



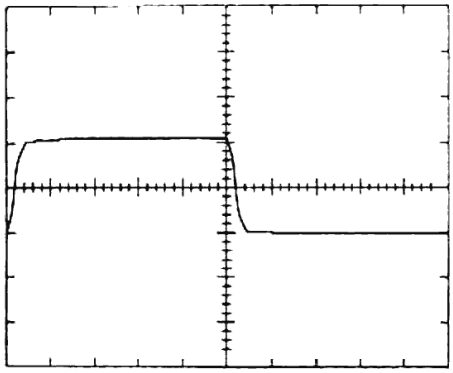
V = 50mV/DIV
H = 100nS/DIV

Small Signal Settling Into 100Ω Load



V = 2V/DIV
H = 100nS/DIV

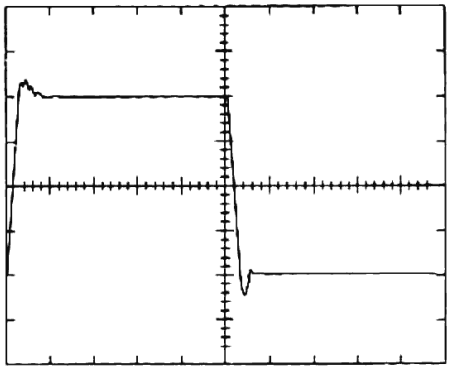
5V Settling Into 1KΩ Load



V = 5V/DIV
H = 100nS/DIV

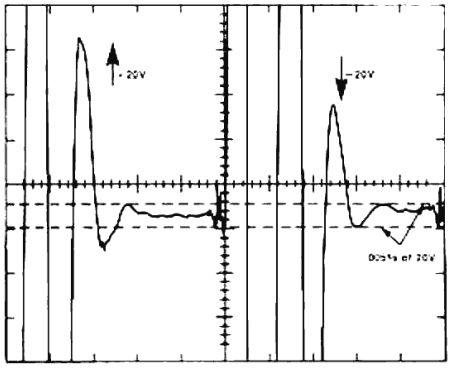
10V Settling Into 1KΩ

The Generator slew rate was purposely limited to 250V/μS to illustrate large signal non-slew settling.



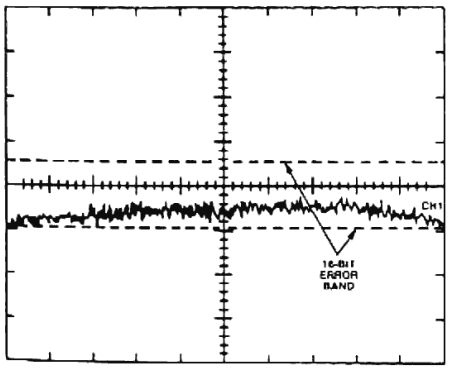
V = 5V/DIV
H = 100nS/DIV

20V Settling Into 1KΩ Load



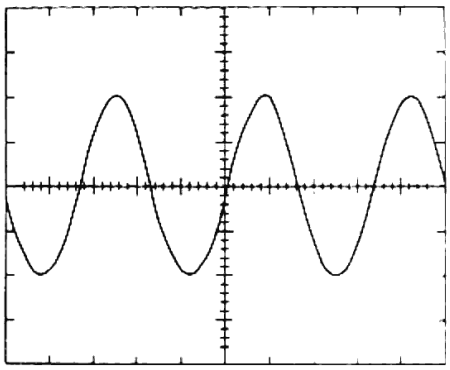
V = 2mV/DIV
H = 100nS/DIV

20V, 0.005% Settling Time Into 1KΩ Load



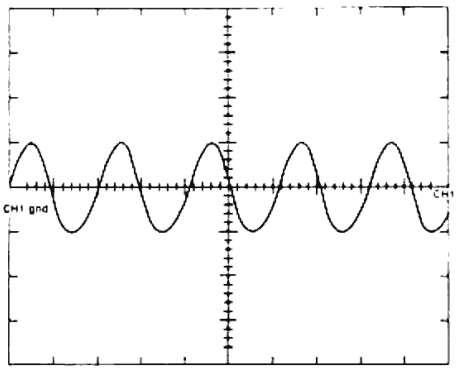
V = 200μV/DIV (V_{out} − V_{in})
H = 2V/DIV (V_{in})

$20V_{p-p}$ Linearity Error With 1KΩ Load



V = 50V/DIV
H = 50nS/DIV

5MHz, 20V Sinewave Into 1KΩ Load



V = 5V/DIV
H = 50nS/DIV

10MHz, 10V Sinewave Into 1KΩ Load

SUPPLY BYPASSING

Power supply bypassing is necessary to prevent oscillation with the SP 4010 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel; adding a 4.7μF solid tantalum capacitor will help in troublesome instances.

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the SP 4010 since it will provide power gain to frequencies over 60 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal lid of the device since it is electrically isolated from internal circuitry. Alternatively, the lid should be connected to the output to minimize input capacitance.

The gain adjust pot and the offset adjust pot should be mounted within one inch of the SP 4010. An etch guard ring should be laid around the gain and offset adjust circuitry and tied to the output to prevent dynamic deterioration from stray capacitance. (See Figure 1).

GAIN AND OFFSET ADJUSTMENTS

In most system applications there will be no need to adjust the gain and offset of the SP 4010 separately. The system gain and offset adjustments could be used instead. However, it is not recommended that the gain and offset adjustment pots connected to the SP 4010 be used to compensate system gain and offset errors.

Figure 1 shows the recommended gain and offset adjustment circuit.

IMPORTANT: The lead length on the gain and offset adjustment circuit should be kept short (within one inch) to avoid oscillation or deterioration of dynamic performance.

The DVM must have both inputs floating. A hand held DVM with 100μV or finer resolution may be used for this measurement.

For very critical adjustments a 5 minute warmup is recommended for the SP 4010.

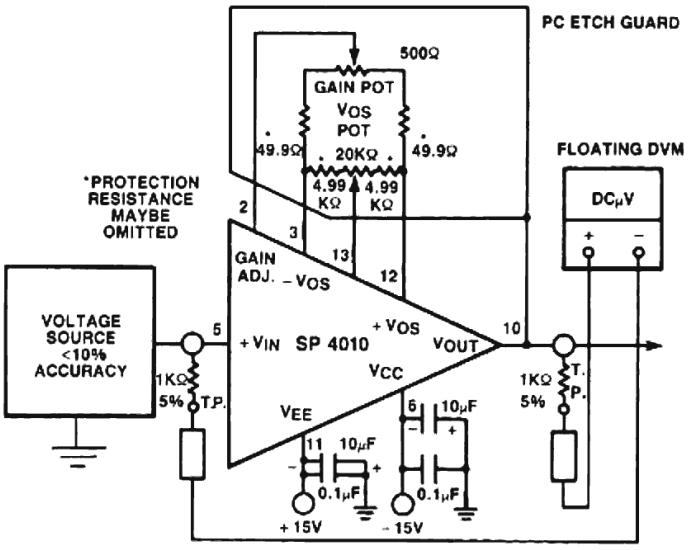


Figure 1. Gain and Offset Adjustment

GAIN ADJUSTMENT

The gain adjustment should be done before the offset adjustment to avoid the effect that the gain pot has on the offset voltage.

The gain adjustment also affects the output resistance of the SP 4010. The output resistance will be closest to zero ohms when the gain is closest to one.

The gain pot is adjusted while plus full scale and minus full scale voltages (as defined by the user's system) are applied to the SP 4010 by an external voltage source or by the previous stage in the system. This applied voltage needs to be only 10% accurate because the floating DVM is measuring gain error directly. The gain error has been compensated when the floating DVM reads the same value for plus full scale and minus full scale input voltages. The input voltage applied to the SP 4010 can be a manually controlled DC voltage or a slow 2 to 10 second period full scale square wave.

OFFSET ADJUSTMENT

After the gain has been adjusted, the remaining error is eliminated by the offset adjustment. The input voltage applied to the SP 4010 should be zero volts. The offset pot is adjusted until the floating DVM reads zero volts.

CAPACITIVE LOADING

Two considerations must be taken into account when driving capacitive loads. These are frequency stability and charge current magnitude.

For some values of load capacitance (>50pf) it may be necessary to isolate the capacitive load with a resistor from 1Ω to 10Ω to reduce ringing or oscillation tendency. The desired step response can be obtained with the right resistor value for each application. (See Figure 2)

The charge current magnitude must be controlled not to exceed the maximum rated output current for the SP 4010. If the maximum output current is exceeded, the output stage will saturate during a transient and will take long to recover.

The charge current into the capacitor is established by

$$I_{C\,load} = C_{load} \times \frac{dv}{dt}$$

The charge current can be limited by controlling the slew rate of the signals driving the SP 4010, by reducing the amount of capacitive loading or by adding resistance in series with the capacitive load.

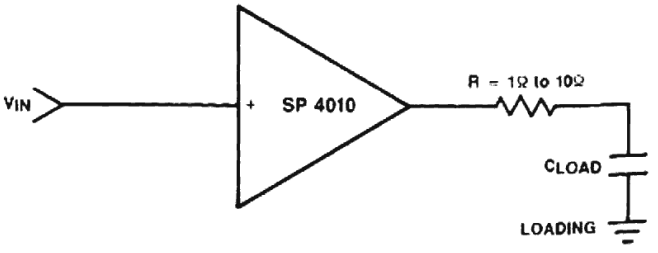


Figure 2. Capacitive Loading

SP 4010 THEORY OF OPERATION

A source follower is a unity gain amplifier that uses field effect transitors in the main signal path. The input is applied at the FET gate, while the output is taken from the FET source. The typical source follower has the advantage of very high input impedance and high speed, but its voltage range, accuracy, linearity and drive capability are poor.

The SP 4010 employs a proprietary architecture that has all the high input impedance and speed of a source follower, as well as the full voltage range, accuracy, linearity and drive capability of a unity gain closed loop op amp.

The SP 4010 is divided into the following circuit blocks: (See simplified schematic on page 1.)

Signal FET Source Follower
Output Buffer Emitter Follower
DC Bias FET and Load Regulation
Bias Current Mirror
Current Feedback Loop (Common Emitter)
Bootstrap

The primary voltage signal path is from the input through the source follower to the emitter follower buffer to the output. The Signal FET Source Follower operates at the channel current set by the Bias FET. The Signal FET source drives the output buffer emitter follower directly through a Vgs shift that cancels its own Vgs.

With matched FET's running at the same ID and Vds, it follows that the offset from gate to gate (or V_{IN} to V_{OUT}) of the FET's is zero.

The Bias Current Mirror and the current feedback common emitter loop adjust the signal FET current until it's matched to the Bias FET current. A residual ID mismatch error remains due to finite gain in the current feedback loop and mirror gain error.

The signal FET is lightly loaded at its source by the finite impedance of the bias current source, output buffer and boot-strapped bias FET current. The current feedback loop is responsible for linearization of the signal FET source voltage under these load currents. The output impedance of the signal FET source is divided by the current gain of the loop.

The DC Bias FET provides not only DC Bias, but also load regulation for the output buffer emitter follower. Any offsets presented by the output buffer simply appear as a minor shift in the Vgs which is common to both FET's and does not affect V_{OUT} vs. V_{IN}.

Any signal dependent variation in the output buffer emitter follower offset as caused by a load resistor or its inherent linearity error, gets transformed into a current by the gm of the Bias FET. This signal flows as a current through the mirror and the current loop forces an equal change in the signal FET current that transforms into an equal and opposite Vgs change with the matched gm of the signal FET.

It is important to note here that the load regulation signal flows through the Bias FET and Mirror once into the current loop without recirculation through the Bias FET.

V_{OUT}/V_{IN} variations on the output buffer emitter follower simply cause a small variation in the operating point of the FET's that is rejected by the CMRR of the FET's.

DC CHARACTERIZATION METHOD

The DC characterization of offset voltage, gain error, linearity, output resistance and output swing under load is done with the test system shown in Figure 3. This test approach was chosen because of it's immunity from source or DVM induced errors.
The SP 4010 unity gain buffer is a 4 terminal device where signal is concerned. There are two power pins, an input pin and an output pin A signal voltage may be applied with respect to ground or with respect to the supplies which are firmly defined with respect to ground. So, except for a signal inversion, it is the same to drive the input with respect to the supplies as it is to drive both supplies with respect to the input.

The latter was chosen and the input of the SP 4010 was grounded so that the supplies may be driven by the DC source DAC 08. This scheme allows direct measure-

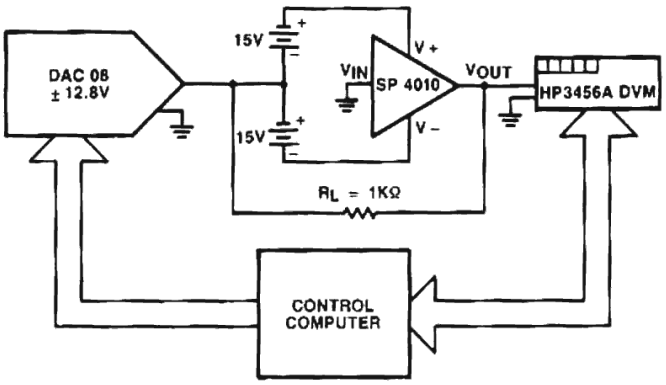


Figure 3. DC Test System

ment of all errors with the HP 3456A DVM, using its more sensitive scales without the resolution and accuracy sacrifice presented by the ± 20V range. The accuracy of the signal source is also very non-critical. The DAC 08 is more than adequate to measure 18-bit linearity on the SP 4010 because the DAC 08 output does not appear in the error signal.

One last point that should be addressed is the distinction between Power Supply rejection ratio and the measurements carried out by this system. Note that while the two 15V "Battery" supplies are being moved with respect to the input pin, each supply is a constant well regulated and bypassed 15V. A power supply rejection ratio test is done by changing the magnitude of the supply voltage individually or by the same amount.

AC CHARACTERIZATION METHOD
STEP RESPONSE

The AC characterization of step response settling time uses the same measurement philosophy as the DC characterization method. The test system is reconfigured by computer control into the test setup shown in Figure 4.

The DAC 08 now controls the amplitude of the square wave that the HI 201HS switches generate. Careful layout and bypassing of all supplies are essential to generate a square wave free of ringing. Any slow droop or amplitude inaccuracy in the square wave is effectively rejected by this measurement method.

The settling error is directly amplified by clamping amplifier and measured on the oscilloscope. As before, there is no need to cancel out the input square wave. The TEKTRONIX 2430 oscilloscope provides hard copy thru a HP 2225A Printer (see Page 3).

FREQUENCY RESPONSE

The frequency response characterization was done with the test system outlined in Figure 5. This test method yields good consistent accurate results with commonly available lab equipment. A small signal (250mV) square wave is fed to the device under test to produce a step response at the output. This square wave must be free of ringing and must have a rise time (= 2nS) that is faster than that of the device under test.

One transition (positive or negative) is captured at the output of the SP 4010, by the TEK 2430 digital storage oscilloscope. The step response is differentiated in the HP 9826 Computer to produce the impulse response. A Fast Fourier Transform is performed on the impulse response to obtain the frequency response. The magnitude of the frequency response is displayed on the CRT and hard copy may be obtained on the printer or plotter. See Page 3 for a copy of the printout.

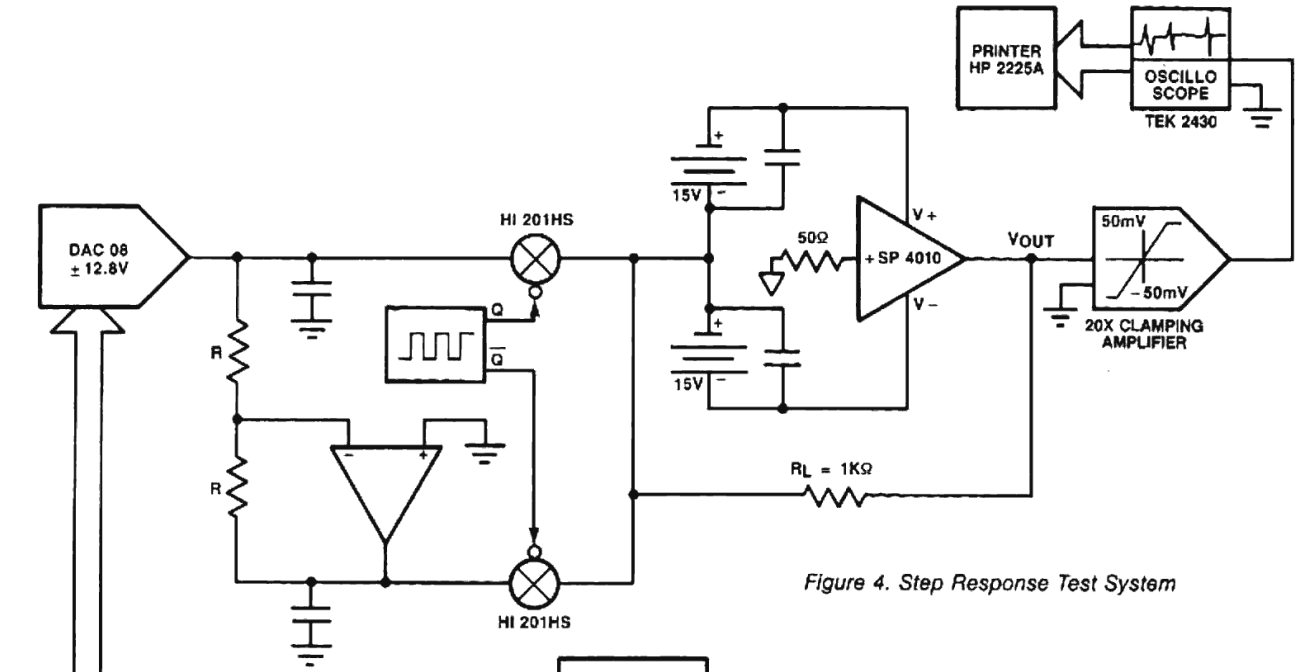


Figure 4. Step Response Test System

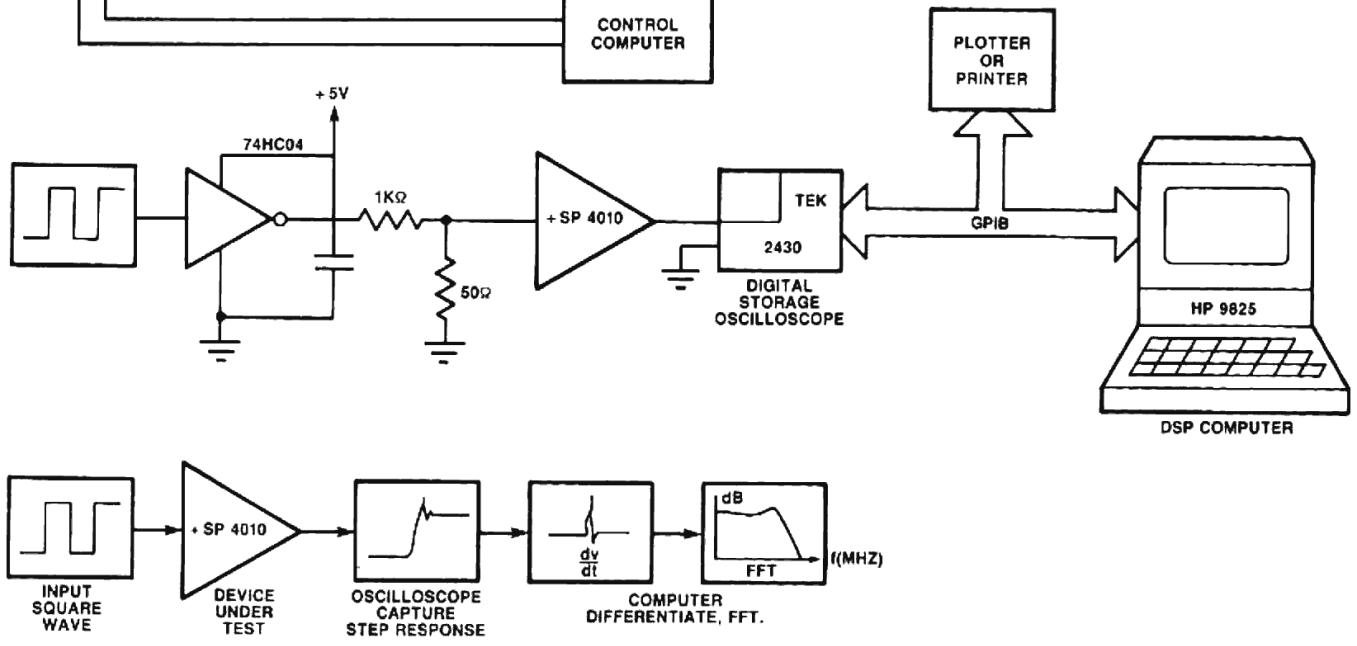
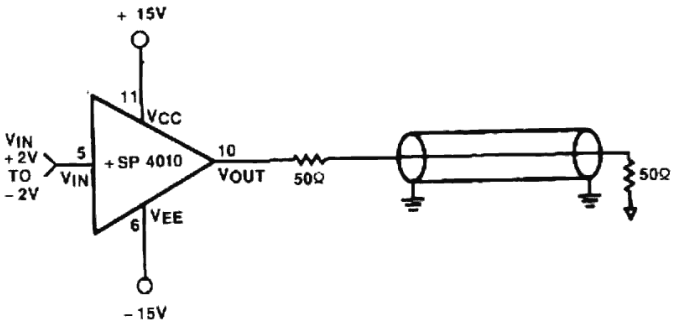
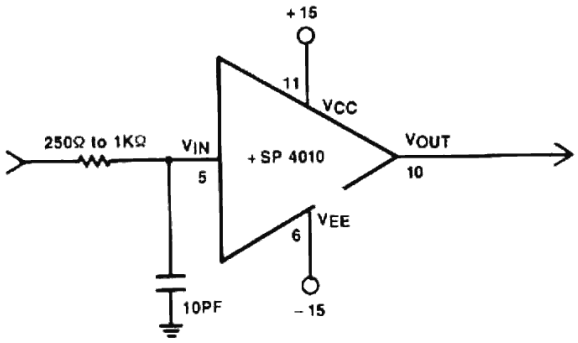


Figure 5. Frequency Response Test System

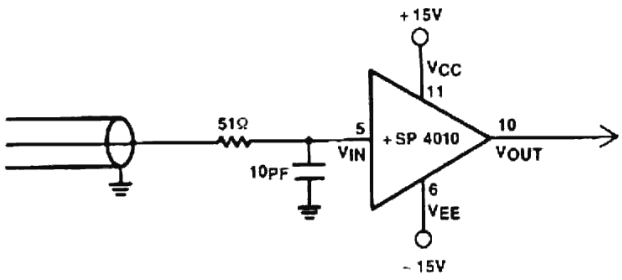
APPLICATION CIRCUITS



PRECISION CABLE DRIVER

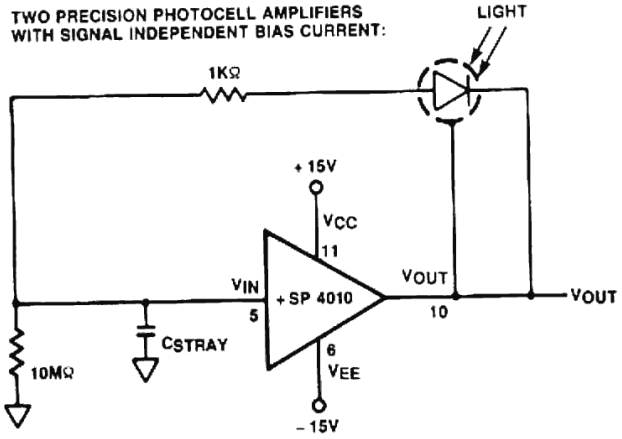


OPTIMIZE FOR LARGE SIGNAL SETTLING



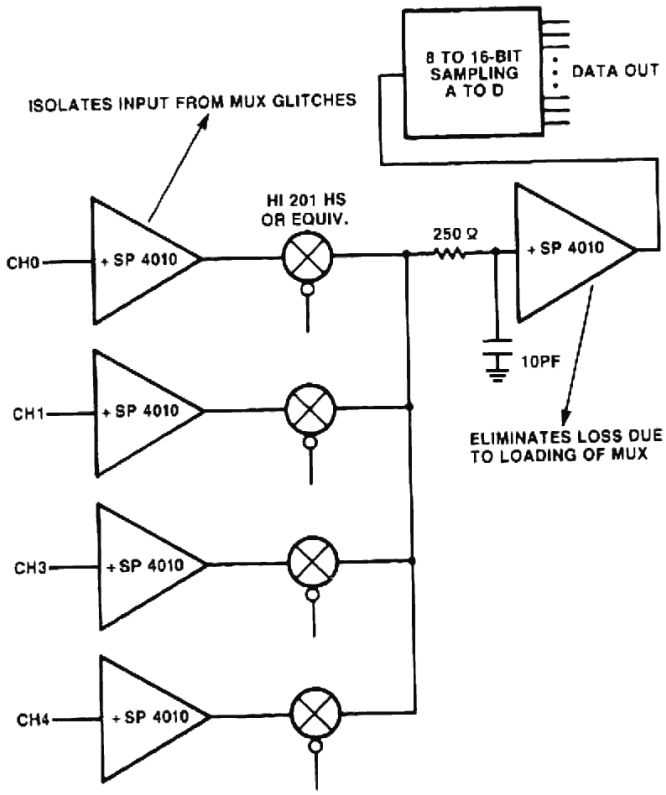
UNTERMINATED CABLE BUFFER

TWO PRECISION PHOTOCELL AMPLIFIERS WITH SIGNAL INDEPENDENT BIAS CURRENT:

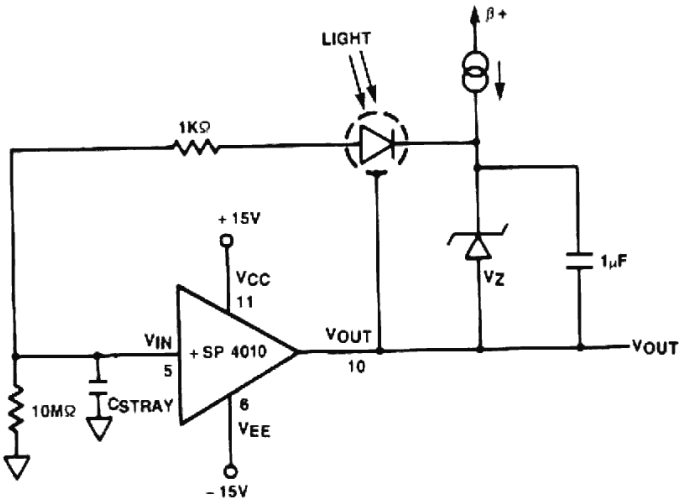


FAST 10MΩ TRANS RESISTANCE AMPLIFIER FOR PHOTO DIODE DETECTOR

$$BW = \frac{1}{2\pi \times 10M\Omega \times C_{STRAY}}$$



VERY HIGH SPEED BUFFERED DAS FOR MAGNETIC RESONANCE IMAGING ON CAT SCANNER APPLICATIONS

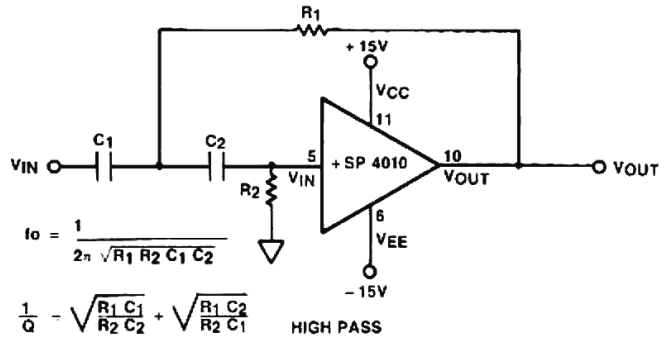


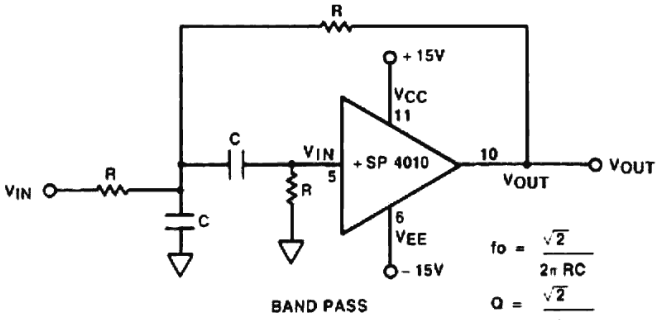
FAST 10MΩTRANS RESISTANCE AMPLIFIER FOR REVERSE BIASED PHOTO DIODE DETECTOR

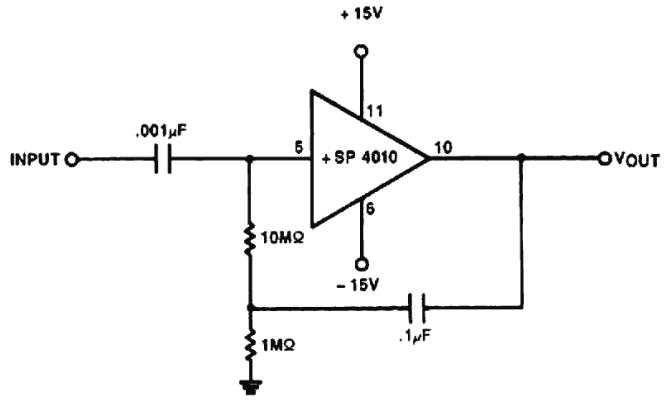
$$BW = \frac{1}{2\pi \times 10M\Omega \times C_{STRAY}}$$

APPLICATION CIRCUITS

Low Distortion Active Filters

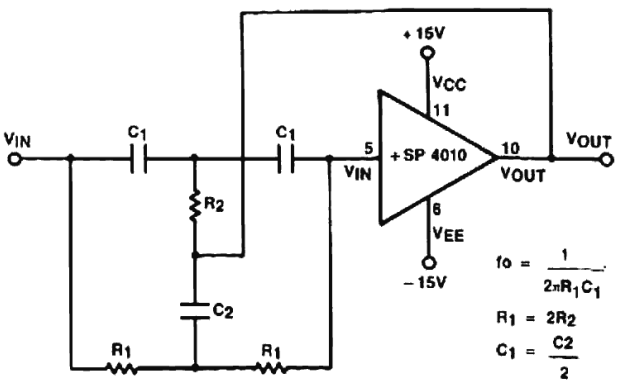


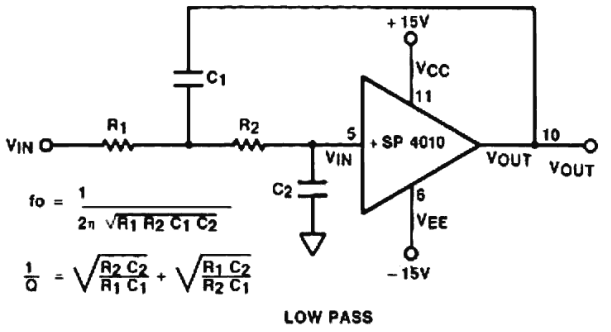


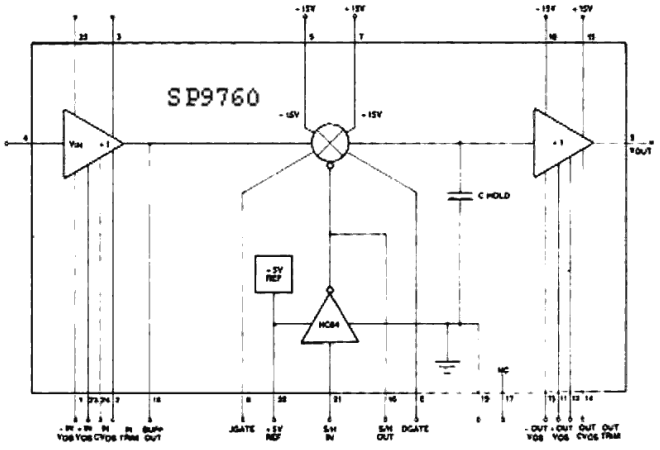


HIGH INPUT IMPEDANCE AC COUPLED AMPLIFIER
BW = 16Hz to 60 MHz . R_{IN} >> 100MΩ

NOTE: REFER TO "RECOMMENDED LAYOUT PRECAUTIONS" FOR ALL APPLICATIONS CIRCUITS







PRECISION HIGH SPEED SAMPLE AND HOLD SP9760