

# 1430/1430-83 200ns TO 0.01% SETTLING, FET OPERATIONAL AMPLIFIERS

Models 1430 and 1430-83 are Hybrid Operational Amplifiers which combine speed, precision, MIL-STD-883 Screening, and 125°C Operation. A guaranteed Settling Time of 200 nano-seconds to 0.01% of Final Value make them ideal output amplifiers for fast 12-bit D/A Converters, fast Sample & Holds, and precision processing of radar pulses.

Their ability to operate within specifications from -55 °C to +125 °C – combined with screening to MIL-STD-883, Method 5008 (as summarized in Table 1) - make them useful in virtually all military applications as well as in severe industrial environments.

**TABLE 1**

Model	Operating Temperature Range	Screened Similar to MIL-STD-883 Method 5008
1430	-55 °C to +125 °C	Internal Visual Stabilization Bake Constant Acceleration Seal, Fine and Gross Leak External Visual
1430-83		Internal Visual Stabilization Bake Constant Acceleration Seal, Fine and Gross Leak Burn-In Temperature Cycling External Visual

It should be noted that settling time does not vary appreciably with closed loop gain. (See Figure 1.) This is particularly important when used as an I to V converter in current DAC's, as shown in Figure 6.

In addition to fast settling, Model 1430 exhibits low bias currents, high slew rate, wide bandwidth, and good phase margin. Although designed primarily for inverting applications, the 1430 will accept up to ±3 Vdc at the non-inverting input for applications requiring an offset. For applications requiring ultra-high speed non-inverting operation, we recommend our Model 1030 or 1435.

Only a feedback capacitor is required for stability at closed-loop gains of unity and above. In applications where the low 2 mV initial offset voltage must be trimmed, an external 1 kΩ potentiometer is used.

### SETTLING TIME – DEFINED

Settling Time is the important specification when handling fast (sub-microsecond rise time), precision (0.1% or better amplitude accuracy) pulses.

Settling Time is defined as the total time required after application of an input step (of voltage or current) for a circuit's output to stay within a specified error band relative to the final value of the output. (See Figure 2)

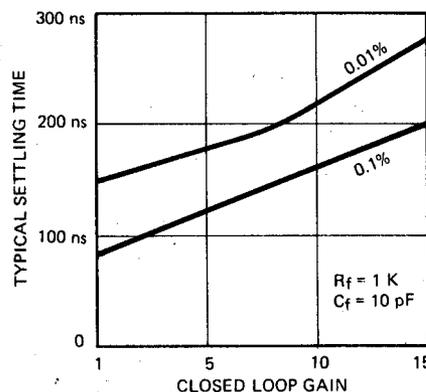


### FEATURES

- 200 nsec Settling Time to 0.01%
- -55 °C to +125 °C Operating Temperature
- Screening similar to MIL-STD-883, Method 5008
- 80 MHz Gain Bandwidth Product
- 500 V/μsec Slew Rate
- ±50 mA Output Current

### APPLICATIONS

- Digital to Analog Converters
- Sample-Hold Circuits
- Pulse Amplifiers
- Wideband Amplifiers



**Figure 1. Settling Time vs Closed Loop Gain**

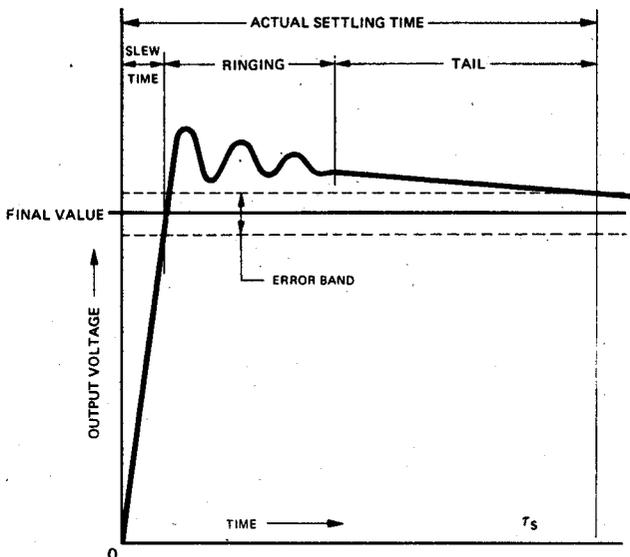


Figure 2. The Composition of Settling Time

Settling time cannot be predicted from bandwidth and/or slewing rate since a step input, when applied to the amplifier, will cause the output to slew at its maximum rate toward the final value. The output will usually overshoot slightly and “ring” as it settles toward the final value.

Settling time, therefore, includes not only the slew rate, but the ringing time as well. The error band is generally expressed as a percentage of the desired output level, i.e., 0.01% or 1 mV for a 10 volt amplifier.

When observing settling time on an oscilloscope the amplifier may appear to have settled (ringing has ceased) but the value is still outside the error band. It may take a few seconds for this to drift within the error band. This phenomenon is called a “long tail” and is often a source of error. The long tails make it virtually impossible to calculate settling time by using slew rate, and ringing characteristics as the

sole factors. It should also be realized that knowing the settling time to a given accuracy (say 0.1%) is in no way helpful in extrapolating the settling time to a higher accuracy such as 0.01% and vice-versa.

If settling time cannot be extrapolated, calculated, guessed, or ignored, it must be measured. This can be a difficult and misleading task if the proper procedures are not followed precisely. Figure 3 illustrates the settling characteristics of the 1430 using the test circuit given in Figure 4A.

**SETTLING TIME – MEASURED**

It is not possible to look for 0.1% or 0.01% accuracy directly from an oscilloscope just by looking at the output waveform. At high sensitivity (for resolution), a 10 volt full scale signal will greatly overdrive the scope’s input amplifier to the point that its recovery time will probably be much worse than the settling time of interest.

The test circuit shown in Figure 4 is an excellent method for fast settling time measurements. In this circuit  $R_{in}$  and  $R_f$  are matched to  $R_{in}'$  and  $R_f'$ . When the AUT\* has settled to  $\pm 0.01\%$  of a 20 V step ( $\pm 2$  mV) the settling point (see Figure 4) will have settled to  $\pm 1$  mV. To minimize capacitance at the settling point an FET follower with less than 1 pF input capacitance (2N5486) is used. The two Schottky Diodes on the settling point act as limiters without storing a charge and also have little capacitive loading effect. Thus the lag due to capacitance (3 pF) in combination with  $R_f = R_i = 1$  k $\Omega$  can be as low as 1.5 nanoseconds.

The diode gate and R1, R2 network forms an ideal square wave source for testing since a square wave with significant ripple can cause (unfairly) an amplifier to look bad. Resistors R1 and R2 can be trimmed for desired output.

This scheme permits you to look quite directly at the true AUT output, yet avoids most of the drawbacks usually entailed because the output signal is subtracted from the input signal.

\*AUT – Amplifier Under Test

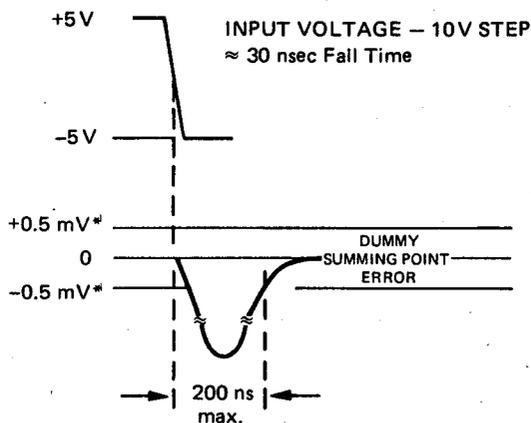
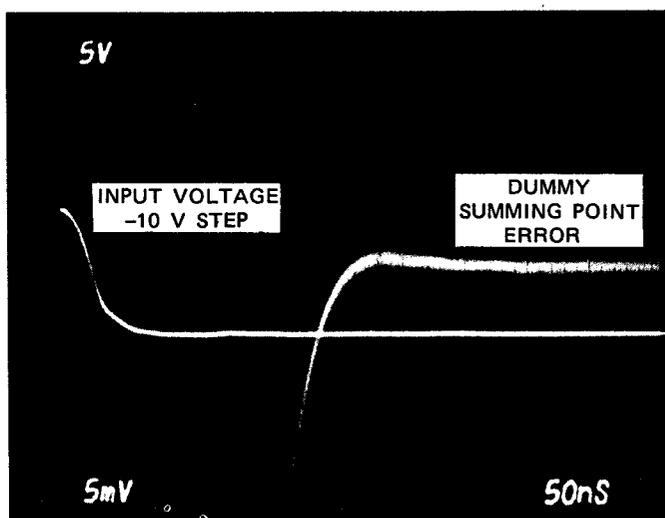


Figure 3. Settling Time of Model 1430/1430-83



See Figure 4 – Test Circuit and Clipping Amplifier. Since the Clipping Amplifier has a gain of 5, 5 mV/division = 1 mV/division on dummy junction. The dummy summing junction has a gain of 1/2, thus settling to 1/2 mV equals 1 mV (0.01%).

Measuring settling time to 0.01% requires a clipping amplifier to prevent overloading the oscilloscope's input. The circuit shown in Figure 4B is excellent for this purpose.

A good question here might be: Why can't you just connect the 2N5486 buffer to the summing point and watch that point settle? There are two good reasons; the feedback capacitance  $C_f$  and the input capacitance  $C_{in}$ . Many fast settling amplifiers give best results when some finite amount of feedback capacitance is used. The effect of this can be seen at the settling point, but not at the summing point. Also, some good amplifiers have significant input capacitance due to "Miller capacitance" or to feedforward capacitors. If this is the case, it is possible to see the true settling only at the settling point. So you can test for settling at the summing point so long as the answer is the same as that at the settling point; but if the answer isn't the same, you shouldn't.

An amplifier is of little use for precision work if its output for a 400 nanosecond pulse rises in 10 nanoseconds (1000 V/ $\mu$ sec slew for 10 V output step), overshoots 20%, rings for 100 nanoseconds, and due to a tail won't arrive permanently within 0.01% of its final value for another 600 nanoseconds. A 1430 will be within 0.01% of final value within 200 nanoseconds.

125°C OPERATION

In order to operate the 1430/1430-83 from +85 to +125°C, it must be used with a 20°C per watt heat sink. A suggested device is the Thermalloy Model 6007A\*, modified as shown in Figure 8 by removing the two fins at each end and adding the aluminum "hold down bar". Heat sink compound must be used between the 1430/1430-83 and the heat sink.

\*2021 West Valley View Lane  
Dallas, Texas 75234

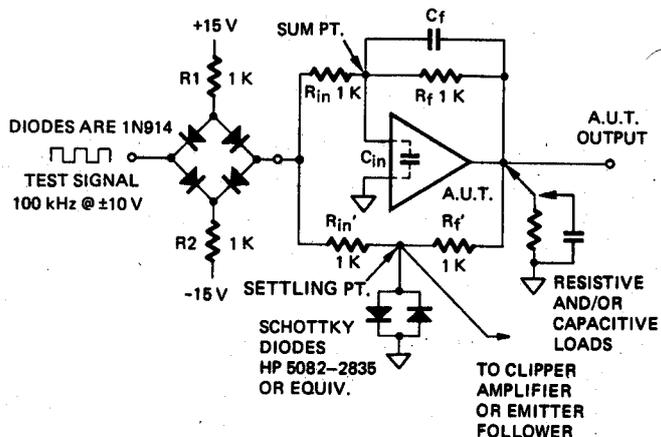


Figure 4A. Test Circuit

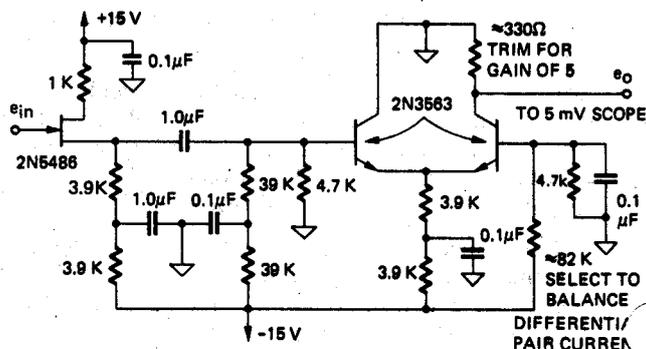


Figure 4B. Clipping Amplifier for 0.01% Measurement

SCREENING SIMILAR TO MIL-STD 883 METHOD 5008		
Test	Methods and Conditions	Purpose
*Internal Visual	Method 2017	Removes potentially defective units with respect to materials, construction, and workmanship.
*Stabilization Bake	Method 1008, Condition C 24 hours at 150°C	Preconditioning treatment to stabilize circuit components prior to conducting further testing and trimming.
*Constant Acceleration	Method 2001, Condition B Y <sub>1</sub> Axis, 10,000 g	Removes potential failures due to weak wire or chip bonding.
*Seal, Fine and Gross	Method 1014, Fine Leak Condition A & C Bomb time 1 hr. at 30 psi; Leak Rate < 5 × 10 <sup>-7</sup> cc/sec; Gross Leak, Condition C <sub>1</sub> , no bubbles	Verifies Integrity of hermetic package
Burn In	Method 1015 Condition B 160 hours at 125°C	Reduces infant mortality rate
Temperature Cycling	Method 1010, Condition B 10 cycles from -55°C +0°C to +125°C +3°C -5°C -0°C	Removes potential failures due to weak wire or chip bonding.
*External Visual	Method 2009	Removes defective units with respect to materials, construction, and workmanship.

\*These tests are standard for both Models 1430 and 1430-83.

**SPECIFICATIONS** Inverting circuits only,  $V_{CC} = \pm 15$  V unless otherwise stated  
(Operation above +85°C requires 20°C/watt heat sink)

	Typical	Guaranteed	Typical
	● +25°C		● -55°C to +125°C
<b>OUTPUT RANGE</b>			
Voltage (Peak)	---	±10 V	±9 V
Current	---	±50 mA	±25 mA
<b>VOLTAGE GAIN (dc, Open Loop)</b>			
Rated Load	114 dB	106 dB	100 dB
<b>FREQUENCY RESPONSE (Inverting Only)</b>			
Small Signal (Gain-Bandwidth Product) ①	100 MHz	80 MHz	50 MHz
Small Signal (Unity Gain Open Loop)	60 MHz	---	---
Max Sine Power Out (3 to 5% distortion)	---	5 MHz	2.5 MHz
Max Peak to Peak Out (Triangle Wave)	---	8 MHz	4.0 MHz
Slew Rate	500 V/μsec	---	500 V/μsec
Setting Time ②	---	---	---
10 V Step to within 100 mV (1%)	70 nsec	---	---
10 mV (0.1%)	100 nsec	---	---
5 V Step to within 50 mV (1%)	70 nsec	---	---
5 mV (0.1%)	100 nsec	---	---
0.5 mV (0.01%)	180 nsec	---	---
2 V Step to within 20 mV (1%)	80 nsec	---	---
2 mV (0.1%)	100 nsec	---	---
0.2 mV (0.01%)	240 nsec	---	---
Overload Recovery Time (10 V Step Input)	10 μsec	---	---
Max Capacitive Load without Oscillation	---	100 pF	50 pF
<b>INPUT VOLTAGE RANGE</b>			
Common Mode for DC Linear Operation	±3 V	---	---
Common Mode Fault	---	±18 V	---
Differential (Between Inputs)	---	36 V	---
<b>INPUT OFFSET VOLTAGE</b>			
Initial (without external trim) @ 25°C	±0.5 mV	±2 mV	---
Zero Adjustment (Optional)	---	1 kΩ pot	---
Vs. Temperature (Avg. -25°C to +85°C)	25 μV/°C	75 μV/°C	100 μV/°C
Power Supply Rejection Ratio	---	3 mV/V	---
<b>INPUT BIAS CURRENT</b>			
Initial @ 25°C	-150 pA	-500 pA	---
Vs. Temperature (Avg. -55°C to 125°C) ③ ④	---	Doubles each 10°C	---
<b>INPUT IMPEDANCE @ dc</b>			
Differential	10 <sup>11</sup> Ω    3 pF	---	---
<b>NOISE (Referred to Input)</b>			
Flicker (0.016 to 1.6 Hz)	---	---	---
Voltage (peak-to-peak)	10 μV	---	---
Current (peak-to-peak)	3 pA	---	---
Midband (1.6 to 160 Hz)	---	---	---
Voltage (rms)	2.5 μV	---	---
Current (rms)	2 pA	---	---
Highband (160 Hz to 16 kHz)	---	---	---
Voltage (rms)	2 μV	---	---
Wideband (1.6 Hz to 1.6 MHz)	---	---	---
Voltage (rms)	9 μV	---	---
<b>POWER REQUIREMENTS</b>			
Nominal Supply Voltage	---	±15 V	---
Voltage Range	±10 to ±18 V	---	---
Current: Quiescent	---	±25 mA	±30 mA
Current: Full Load	---	±75 mA	---
<b>TEMPERATURE RANGE</b>			
Operating ⑤	---	-55°C to +125°C	---
Storage	---	-65°C to +150°C	---
<b>MTBF @ 85°C ⑥</b>			
			> 694,000 hrs

- ① @ 1 MHz (See circuit of Figure 4A)
- ②  $R_i = R_f = 1$  kΩ  
 $C_f = 15$  pF for 0.01%, 10 pF for 0.1%  
 $R_L = 250$  Ω  $C_L = 10$  pF
- ③ Bias Current @ +85°C is 10 nA, max.  
Bias Current @ +125°C is 1 μA, max.
- ④ With 20°C/watt heat sink above 85°C (see Figure 8).
- ⑤ Ground Benign Per Mil Handbook 217B

The input circuits of these units are protected to  $\pm V_{CC}$ . Output circuits are short-circuit protected to ground.

Recommended Power Supply: Teledyne Philbrick Model 2211

Teledyne Philbrick makes no representation that use of its modules in the circuits described herein, or use of other technical information contained herein will not infringe on existing or future patent rights nor do the descriptions contained herein imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith.



Allied Drive at Route 128, Dedham, Massachusetts 02026  
Tel: (617) 329-1600 TWX: (710) 348-6726 Telex: 92-4439

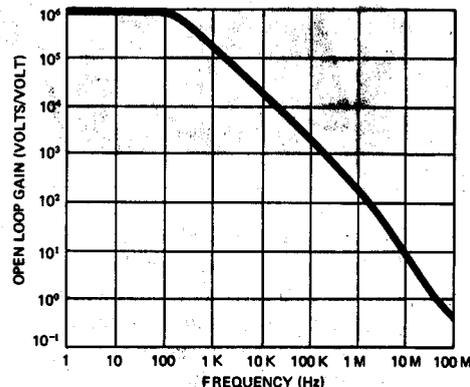


Figure 5. Open Loop Gain vs Frequency

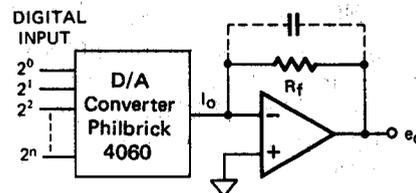


Figure 6. Output Amplifier for D/A Converter

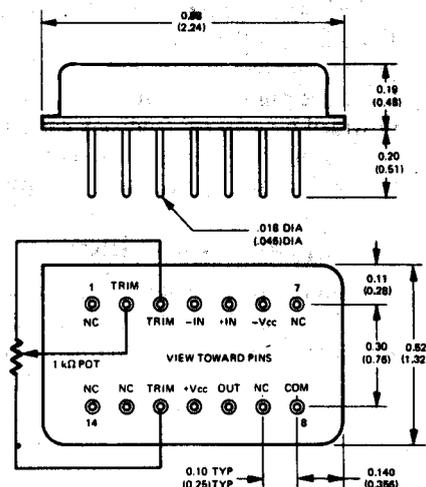
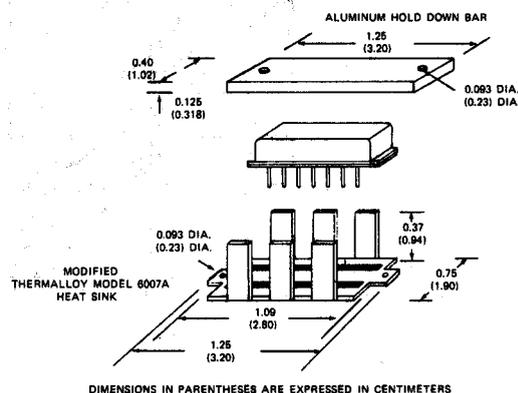


Figure 7. Mechanical Configuration



DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS

Figure 8. 1430/1430-83 Heat Sink Assembly