

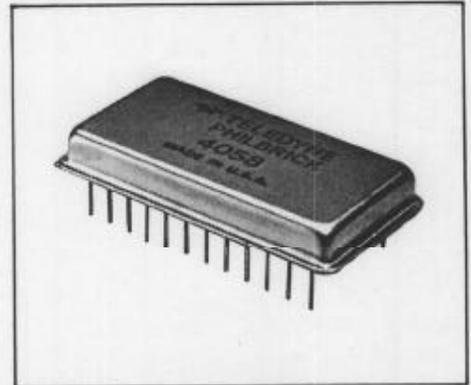
Fast, 12 Bit High reliability D/A Converter

The 4058 is a true 12 bit digital to analog converter with TTL compatible inputs. It has user programmable output voltage ranges of 0 to -5V, 0 to -10V, $\pm 2.5V$, $\pm 5V$, and $\pm 10V$ and output current ranges of 0 to +4mA and $\pm 2mA$. It is one of the fastest settling D/A's available, guaranteeing output settling to $\pm \frac{1}{2}LSB$ in $2.5\mu sec$ for a 20V step and 200 nsec for a 4mA step. The standard 4058 is fully specified for $0^{\circ}C$ to $+70^{\circ}C$ operation. The 4058-83 guarantees full performance over the $-55^{\circ}C$ to $+125^{\circ}C$ temperature range and is screened to the high reliability requirements of MIL-STD-883, Method 5008.

The 4058 D/A converter is a thin-film hybrid that combines a proprietary, dielectrically isolated switching network; a specially designed, low capacitance, thin-film, chromium cobalt resistor network; a high speed output amplifier; and a carefully buffered zener diode reference. The switching network uses an emitter coupled logic approach. Its speed, the speed of the output op amp, and the low capacitance of the resistor network are responsible for the 4058's ability to settle a full 20V step to $\pm 0.01\%$ FSR in $2.5\mu sec$ maximum. The excellent stability of the chromium cobalt thin film enables the 4058 to guarantee monotonicity over its entire operating temperature. The carefully buffered reference gives the 4058 an outstanding PSSR.

The 4058 is packaged in an industry-standard, hermetically sealed, metal dual-in-line package. Active laser trimming results in integral and differential linearity errors guaranteed not to exceed $\pm \frac{1}{2}LSB$. For the most critical applications, external gain and offset adjustments are user optional. The 4058 operates from $\pm 15V$ supplies with no need for a +5V logic supply. Power consumption, at 645mW maximum, is extremely low for a device of this speed. The 4058-83's speed, excellent glitch characteristics, guaranteed temperature performance, and excellent track record for reliability and durability have made it the most popular D/A converter for military/aerospace display applications.

4058



FEATURES

- Fast Settling to $\pm 0.01\%$
 $2.5\mu sec$ Max 20V Step
200nsec Max 4mA Step
- $\pm \frac{1}{2}LSB$ Max Integral and Differential Nonlinearities
- Monotonicity Guaranteed Over Temperature
- Power Consumption 645mW Max
- $-55^{\circ}C$ to $+125^{\circ}C$ Operation
- Optional Screening to MIL-STD-883, Method 5008

APPLICATIONS

- Military Environments
- High Reliability Industrial Equipment
- Data Distribution Systems
- Precision Displays
- Portable Instrumentation

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ABSOLUTE MAXIMUM RATINGS

+ 15V Supply (+ V_{CC}, Pin 21)
 - 15V Supply (- V_{CC}, Pin 23)
 Digital Input Voltage (Pins 1-12)
 Output Short Circuit Duration (Note 1)
 Operating Temperature Range
 Specified Temperature Range
 4058
 4058-83 (Note 2)
 Storage Temperature Range

+ 18 Volts
 - 18 Volts
 0 to +7 Volts
 Continuous to Ground
 - 55°C to + 125°C
 0°C to + 70°C
 - 55°C to + 125°C
 - 65°C to + 150°C

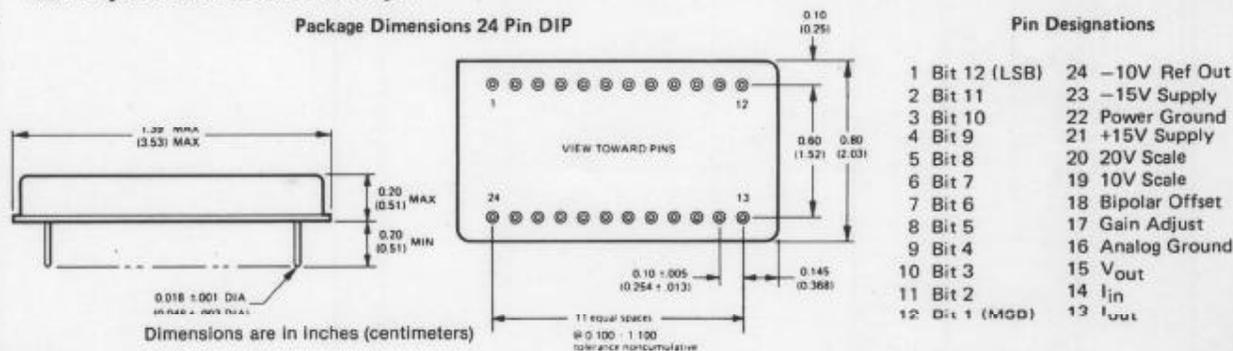
SPECIFICATIONS (T_A = + 25°C, ± V_{CC} = ± 15V unless otherwise indicated).

PARAMETER	MIN.	TYP.	MAX.	UNITS
DIGITAL INPUTS				
Logic Levels: Logic "1" Logic "0"	+ 2.0 0		+ 5.5 + 0.8 1	Volts Volts TTL Load
Loading (Note 3) Logic Coding (Note 4): Voltage Output Current Output		GBIN, COB BIN, OBIN		
ANALOG OUTPUT				
Voltage: Ranges Unipolar Ranges Bipolar Output Current Output Resistance Short Circuit Current (Note 1) Max. Capacitive Load	± 5	0 to - 5, 0 to - 10 ± 2.5, ± 5, ± 10 ± 20 0.05 ± 25 50		Volts Volts mA Ω mA pF
Current: Range Unipolar Range Bipolar Output Resistance Unipolar Output Resistance Bipolar Compliance Voltage	± 0.6	0 to + 4 ± 2 1.5 1.2		mA mA kΩ kΩ Volts
TRANSFER CHARACTERISTICS				
Integral Linearity Error: + 25°C 0°C to + 70°C (4058) - 55°C to + 125°C (4058-83)		± ¼ ± ½ ± ½	± ½	LSB LSB LSB
Differential Linearity Error		± ¼	± ½	LSB
Guaranteed Monotonicity: 4058 4058-83	0 - 50		+ 70 + 120	°C °C
Zero Offset Error (Note 5): Voltage Output: Unipolar (000...000) Bipolar (100...000) Current Output: Unipolar (000...000) Bipolar (100...000)		± 1 ± 1 ± ¼ ± ¼	± 4 ± 4 ± ½ ± ½	LSB LSB LSB LSB
Gain Error (Notes 5, 6): Voltage Output Current Output		± 0.05 ± 0.1	± 0.2 ± 1	% %
STABILITY				
Zero Offset Drift Voltage Output: Unipolar Bipolar Current Output: Unipolar Bipolar		± 3 ± 10 ± 0.5 ± 5	± 15 ± 25 ± 1 ± 10	ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C
Gain Drift: Voltage Output Current Output		± 10 ± 7	± 20 ± 20	ppm/°C ppm/°C
Reference Drift		± 5	± 15	ppm/°C
Power Supply Rejection Ratio		± 0.001	± 0.0024	%FSR/%V _S
Warm Up Time to within ± 1LSB		30		Seconds
DYNAMIC CHARACTERISTICS				
Settling Time to ± ½LSB Voltage Output: 5V Step 10V Step 20V Step Current Output, 4mA Step		1.2 1.2 1.9 150	2 2 2.5 200	μsec μsec μsec nsec
Slew Rate		16		V/μsec

PARAMETER	MIN.	TYP.	MAX.	UNITS
REFERENCE				
Voltage		- 10.0		Volts
Accuracy		± 1		%
External Load			2	mA
POWER SUPPLIES				
Range		± 2		%
Current Drain: +15V Supply		+ 20	+ 25	mA
- 15V Supply		- 13	- 18	mA
Power Consumption		495	645	mW

SPECIFICATION NOTES

- The 4058's current and voltage outputs can withstand continuous shorts to ground. The reference output (pin 24) can withstand a short for approximately 2 seconds.
- The 4058-83 is fully specified for - 55 to + 125°C operation and screened to the high reliability requirements of MIL-STD-883, Method 5008.
- A TTL load is defined as sinking 40µA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
- CBIN = Complementary Binary. COB = Complementary Offset Binary. BIN = Binary (straight binary). OBIN = Offset Binary. See Digital Coding Table.
- Adjustable to zero with optional external trim potentiometer.
- Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output voltage/current span from the 0000 0000 0000 output to the 1111 1111 1111 output.



Applications Information

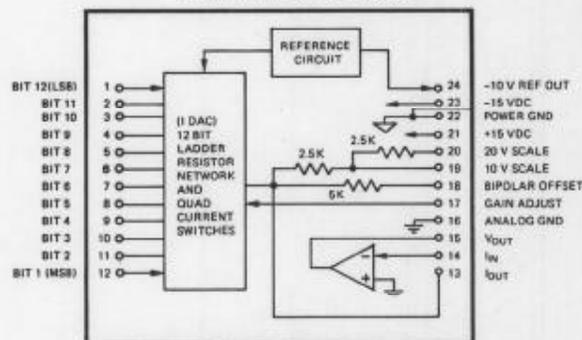
Grounding and Bypassing

High speed systems require added care in power distribution for maximum accuracy and speed. Although power supply inputs on the 4058 are internally bypassed with 0.01µF ceramic capacitors, it is recommended that an additional 1µF tantalum capacitor be added externally between each supply input and analog ground for optimum performance. It is important to realize that power ground (pin 22) is internally connected to the case and must be connected to system analog ground to minimize ground loop errors. It is preferable to have the 4058's analog and power ground pins soldered directly to a large analog ground plane beneath the 4058.

Optimizing Settling Time

To optimize settling time of the 4058 and to make the settling time independent of the characteristics of the digital driver, 2.2kΩ 1/8 Watt pulldown resistors are recommended at all logic inputs.

Functional Block Diagram



Analog ground and power ground must be externally connected to each other. Power ground is connected to case. All units are supplied with a mylar insulator for isolation between the case and pc board.

Logic Inputs

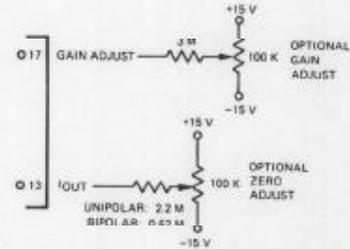
Logic inputs are standard TTL/DTL compatible. If any bits are not used, it is recommended they be grounded since an "open" bit input line is equivalent to a logic "1". Opening the bit lines should not, however, be used as a means of

generating a logic "1" due to the possibilities of noise pickup. The table below shows the binary input code used by the 4058. If desired, virtually any other binary code can be used with the addition of the necessary external logic.

Analog Output		Digital Input	
Voltage	Current	Unipolar Binary	Bipolar Offset Binary
+ F.S.	- F.S.		000...000
+ ½ F.S.	- ½ F.S.		010...000
+ 1LSB	- 1LSB		011...111
0	0	000...000	100...000
- 1LSB	+ 1LSB	000...001	100...001
- ½ F.S.	+ ½ F.S.	100...000	110...000
- F.S. + 1LSB	+ F.S. - 1LSB	111...111	111...111

Trim Procedures

Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the diagram below. Adjustments should be made following warm-up, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature.



Zero Adjustment—For voltage output operation, set the digital input code to 000...000; and adjust the offset trim potentiometer for zero output voltage (unipolar) or plus full scale output voltage (bipolar). For current output operation, set the digital input code to 000...000, and adjust the offset trim potentiometer for zero output current (unipolar) or minus full scale output current (bipolar).

Gain Adjustment—For voltage output operation, set the digital input code to 111...111, and adjust the gain trim potentiometer for minus full scale plus 1LSB output voltage. For current output operation, set the digital input code to 111...111, and adjust the gain trim potentiometer for plus full scale minus 1LSB output current.

Output

Pin Programming

Output Range	Output Pin	Jumper Pin 14 to	Jumper Pin 18 to	Jumper Pin 19 to	Jumper Pin 20 to
0 to -5V	Pin 15	Pin 13	Pin 16 (ground)	Pin 15	Pin 13
0 to -10V	Pin 15	Pin 13	Pin 16 (ground)	Pin 15	_____
± 2.5V	Pin 15	Pin 13	Pin 24	Pin 15	Pin 13
± 5V	Pin 15	Pin 13	Pin 24	Pin 15	_____
± 10V	Pin 15	Pin 13	Pin 24	_____	Pin 15
0 to +4mA	Pin 13	Pin 15 (Note)	_____	_____	_____
± 2mA	Pin 13	Pin 15 (Note)	Pin 24	_____	_____

Note: If oscillations or ringing occur, connect a 100kΩ resistor between pins 14 and 15.

Screening According to MIL-STD-883, Method 5008

Test	Methods and Conditions	Purpose
Internal Visual	Method 2017	Removes potentially defective units with respect to materials, construction, and workmanship.
Stabilization Bake	Method 1008, Condition C 24 hours at 120°C	Preconditioning treatment to stabilize circuit components prior to conducting further testing and trimming.
Constant Acceleration	Method 2001, Condition B Y ₁ Axis, 10,000 g	Removes potential failures due to weak wire or chip bonding.
Seal, Fine and Gross	Method 1014, Fine Leak Condition A & C Bomb time 1 hour at 30 psi; Leak Rate < 5 × 10 ⁻⁷ cc/sec; Gross Leak, Condition C ₁ , no bubbles	Verifies integrity of hermetic package.
Burn In	Method 1015, Condition B 168 hours at 125°C	Reduces infant mortality rate.
Temperature Cycling	Method 1010, Condition B 10 cycles from -55°C +0°C to +125°C +3°C -5°C -0°C	Removes potential failures due to weak wire or chip bonding.
External Visual	Method 2009	Removes defective units with respect to materials, construction, and workmanship.