TELEDYNE PHILBRICK

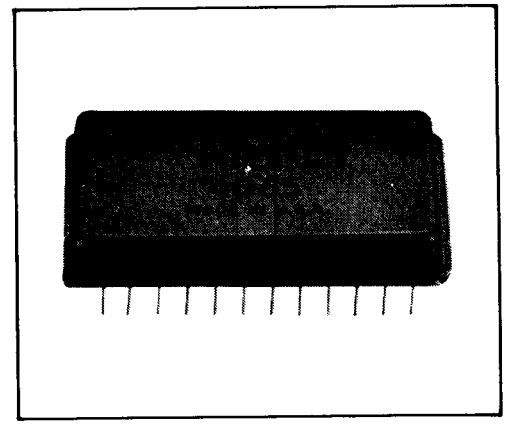
12 Bit, 60nsec Current Output D/A Converter

4065

The 4065 is a true 12 bit, straight binary, current-output digital to analog converter with TTL compatible inputs and externally programmable output ranges of 0 to +4mA and ±2mA. The standard 4065 is fully specified for 0°C to +70°C operation. The 4065-83 guarantees full performance over the −55°C to +125°C temperature range and is screened to the high reliability requirements of MIL-STD-883, Method 5008.

The 4065 D/A converter is a thin-film hybrid that combines a proprietary, dielectrically isolated switching network, a specially designed, low capacitance, thin-film, chromium cobalt resistor network, and a carefully buffered zener diode reference. The switching network uses an emitter coupled logic approach. Its speed and the low capacitance of the resistor network are responsible for the 4065's ability to settle a full 4mA step to ±0.01%FSR in 100nsec maximum. The excellent stability of the chromium cobalt thin film enables the 4065 to guarantee monotonicity over its entire operating temperature range (including the −55°C to +125°C model). The carefully buffered low drift reference gives the 4065 a low gain drift of ±7ppm/°C and an outstanding PSRR of ±0.0024%FSR/%Vs maximum (equivalent to ±0.67 LSB's/Volt).

The 4065 is packaged in an industry-standard, hermetically sealed, metal, 24 pin dual-in-line package. Active laser trimming results in integral and differential linearity errors guaranteed not to exceed ±½LSB and an initial offset error no greater than ±½LSB. For the most critical applications, external gain and offset adjustments are user optional. The 4065 operates from ±15V supplies with no need for a +5V logic supply. Power consumption, at 645mW maximum, is extremely low for a device of this speed.



FEATURES

- 60nsec Settling 4mA Step to ±½LSB
- ±½LSB Max Integral and Differential Nonlinearities
- Monotonicity Guaranteed Over Temperature
- Power Consumption 645mW Max
- −55°C to +125°C Operation
- Optional Screening to MIL-STD-883, Method 5008

APPLICATIONS

- Military Environments
- High Reliability Industrial Equipment
- Data Distribution Systems
- Fast A to D Converters
- Precision Displays
- Portable Instrumentation

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ABSOLUTE MAXIMUM RATINGS

+ 15V Supply (+ V_{CC}, Pin 21)	+ 18 Volts
- 15V Supply (- V_{CC}, Pin 23)	- 18 Volts
Digital Input Voltage (Pins 1-12)	0 to + 7 Volts
Output Short Circuit Duration (Note 1)	Continuous to Ground
Operating Temperature Range	- 55°C to + 125°C
Specified Temperature Range	
4065	0°C to + 70°C
4065-83 (Note 2)	- 55°C to + 125°C
Storage Temperature Range	- 65°C to + 150°C

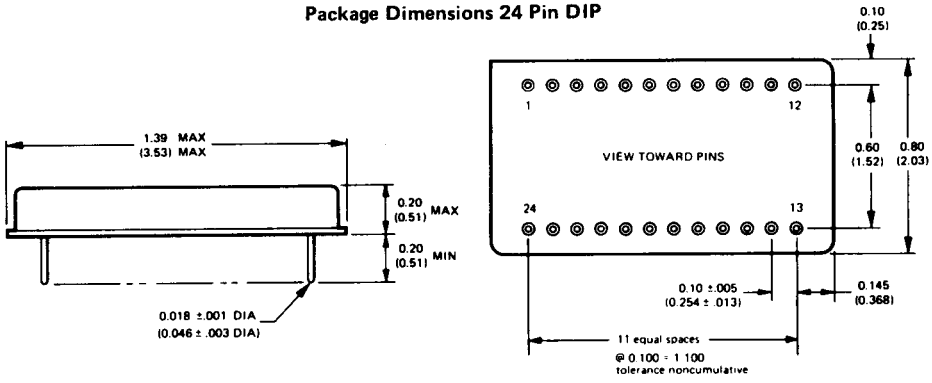
SPECIFICATIONS (T_A = + 25°C, ± V_{CC} = ± 15V unless otherwise indicated).

PARAMETER	MIN.	TYP.	MAX.	UNITS
DIGITAL INPUTS				
Logic Levels: Logic "1"	+ 2.0		+ 5.5	Volts
Logic "0"	0		+ 0.8	Volts
Loading (Note 3)			1	TTL Load
Logic Coding: Unipolar Range		Straight Binary		
Bipolar Range		Offset Binary		
ANALOG OUTPUT				
Output Range: Unipolar		0 to + 4		mA
Bipolar		± 2		mA
Compliance Voltage	± 0.6			Volts
Output Resistance: Unipolar		1.5		kΩ
Bipolar		1.2		kΩ
TRANSFER CHARACTERISTICS				
Integral Linearity Error: + 25°C		± ¼	± ½	LSB
0 to + 70°C (4065)		± ½		LSB
- 55°C to + 125°C (4065-83)		± ½		LSB
Differential Linearity Error		± ¼	± ½	LSB
Guaranteed Monotonicity: 4065	0		+ 70	°C
4065-83	- 55		+ 125	°C
Zero Offset Error (Note 4): Unipolar (000...000)		± ¼	± ½	LSB
Bipolar (100...000)		± ¼	± ½	LSB
Gain Error (Notes 4, 5)		± 0.1	± 1	%
STABILITY				
Zero Offset Drift: Unipolar		± 0.5	± 1	ppm of FSR/°C
Bipolar		± 3	± 10	ppm of FSR/°C
Gain Drift		± 7	± 20	ppm/°C
Reference Drift		± 5	± 15	ppm/°C
Power Supply Rejection Ratio		± 0.001	± 0.0024	%FSR/%Vs
Warm Up Time to within ± 1LSB		30		Seconds
DYNAMIC CHARACTERISTICS				
Settling Time (4mA step to ± ½LSB)		60	100	nsec
REFERENCE				
Voltage		- 10.0		Volts
Accuracy		± 1		%
External Load			2	mA
POWER SUPPLIES				
Range		± 2		%
Current Drain: + 15V Supply		+ 20	+ 25	mA
- 15V Supply		- 13	- 18	mA
Power Consumption		495	645	mW

SPECIFICATION NOTES

1. The 4065's output can withstand a continuous short to ground. The reference output (pin 24) can withstand a short for approximately 2 seconds.
2. The 4065-83 is fully specified for - 55 to + 125°C operation and screened to the high reliability requirements of MIL-STD-883, Method 5008.
3. A TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
4. Adjustable to zero with optional external trim potentiometer.
5. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output current span from the 0000 0000 0000 output to the 1111 1111 1111 output.

Package Dimensions 24 Pin DIP



Dimensions are in inches (centimeters)

Pin Designations

1	Bit 12 (LSB)	24	−10V Ref Out
2	Bit 11	23	−15V Supply
3	Bit 10	22	Power Ground
4	Bit 9	21	+15V Supply
5	Bit 8	20	20V Scale
6	Bit 7	19	10V Scale
7	Bit 6	18	Bipolar Offset
8	Bit 5	17	Gain Adjust
9	Bit 4	16	Analog Ground
10	Bit 3	15	N/C
11	Bit 2	14	N/C
12	Bit 1 (MSB)	13	I_{out}

Applications Information

Grounding and Bypassing

High speed systems require added care in power distribution for maximum accuracy and speed. Although power supply inputs on the 4065 are internally bypassed with 0.01μF ceramic capacitors, it is recommended that an additional 1μF tantalum capacitor be added externally between each supply input and analog ground for optimum performance. It is important to realize that power ground (pin 22) is internally connected to the case and must be connected to system analog ground to minimize ground loop errors. It is preferable to have the 4065's analog and power ground pins soldered directly to a large analog ground plane beneath the 4065.

Logic Inputs

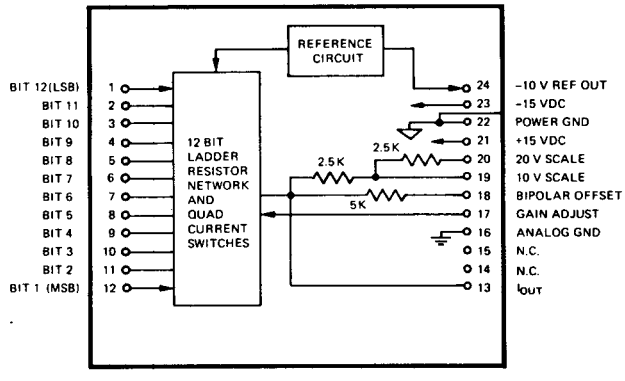
Logic inputs are standard TTL/DTL compatible. If any bits are not used, it is recommended they be grounded since an "open" bit input line is equivalent to a logic "1". Opening the bit lines should not, however, be used as a means of generating a logic "1" due to the possibilities of noise pickup. The table below shows the binary input code used by the 4065. If desired, virtually any other binary code can be used with the addition of the necessary external logic.

Output Range Selection

The table below shows pin connections for 4065 output range selection.

Output		Pin Programming
Output Range	Output Pin	Jumper Pin 18 to
0 to +4mA	Pin 13	———
±2mA	Pin 13	Pin 24

Functional Block Diagram



Analog ground and power ground must be externally connected to each other. Power ground is connected to case. All units are supplied with a mylar insulator for isolation between the case and pc board.

Optimizing Settling Time

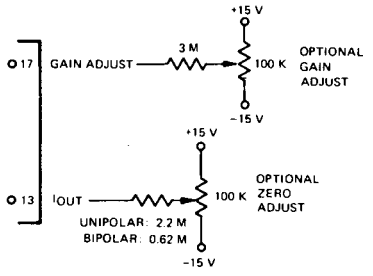
To optimize settling time of the 4065 and to make the settling time independent of the characteristics of the digital driver, 2.2kΩ 1/8 Watt pulldown resistors are recommended at all logic inputs.

Digital Input Coding

Analog Output	Digital Input	
Current	Unipolar Binary	Bipolar Offset Binary
−F.S.		000...000
−½F.S.		010...000
−1LSB		011...111
0	000...000	100...000
+1LSB	000...001	100...001
+½F.S.	100...000	110...000
+F.S. − 1LSB	111...111	111...111

Trim Procedures

Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the diagram below. Adjustments should be made following warm-up, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature.



Offset Adjustment—When utilizing the internal feedback resistors with an external amplifier, set the digital input code to 000...000, and adjust the offset trim potentiometer for zero voltage (unipolar) or plus full scale voltage (bipolar) at the amplifier output. For current output operation, set the digital input code to 000...000, and adjust the offset trim potentiometer for zero output current (unipolar) or minus full scale output current (bipolar).

Gain Adjustment—When utilizing the internal feedback resistors with an external amplifier, set the digital input code to 111...111, and adjust the gain trim potentiometer for minus full scale plus 1LSB voltage at the amplifier output. For current output operation, set the digital input code to 111...111, and adjust the gain trim potentiometer for plus full scale minus 1LSB output current.

Screening According to MIL-STD-883, Method 5008

Test	Methods and Conditions	Purpose
Internal Visual	Method 2017	Removes potentially defective units with respect to materials, construction, and workmanship.
Stabilization Bake	Method 1008, Condition C 24 hours at 150°C	Preconditioning treatment to stabilize circuit components prior to conducting further testing and trimming.
Constant Acceleration	Method 2001, Condition B Y_1 Axis, 10,000 g	Removes potential failures due to weak wire or chip bonding.
Seal, Fine and Gross	Method 1014, Fine Leak Condition A & C Bomb time 1 hour at 30 psi; Leak Rate $< 5 \times 10^{-7}$ cc/sec; Gross Leak, Condition C_1, no bubbles	Verifies integrity of hermetic package.
Burn In	Method 1015, Condition B 168 hours at 125°C	Reduces infant mortality rate.
Temperature Cycling	Method 1010, Condition B 10 cycles from $-55°C\ ^{+0°C}_{-5°C}$ to $+125°C\ ^{+3°C}_{-0°C}$	Removes potential failures due to weak wire or chip bonding.
External Visual	Method 2009	Removes defective units with respect to materials, construction, and workmanship.

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