TELEDYNE PHILBRICK

Monolithic 12 Bit, High Speed D/A Converter

4068

The 4068 is a monolithic, current-output 12 bit D/A converter that combines high speed settling and true 12 bit performance on a single chip. A full 5mA output step settles to ± 0.01%FSR (± ½LSB) in 300nsec typical, 400nsec maximum. Maximum integral and differential linearity errors are guaranteed less than ± ½LSB, and monotonicity is guaranteed over the 4068's entire 0°C to + 70°C operating temperature range. The 4068 is packaged in a hermetically sealed, 24 pin dual-in-line package. Laser trimmed thin-film resistors account for the device's outstanding stability. Gain and offset drifts are guaranteed less than ± 10ppm/°C and ± 2ppm of FSR/°C respectively.

The 4068 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data distribution systems requiring throughput rates as high as 3.3MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed and/or high resolution industrial process control systems.

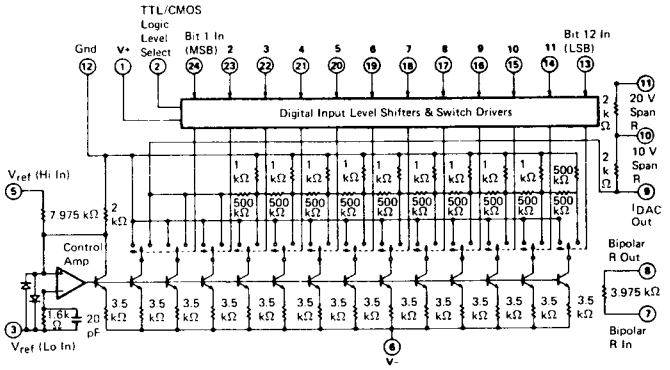
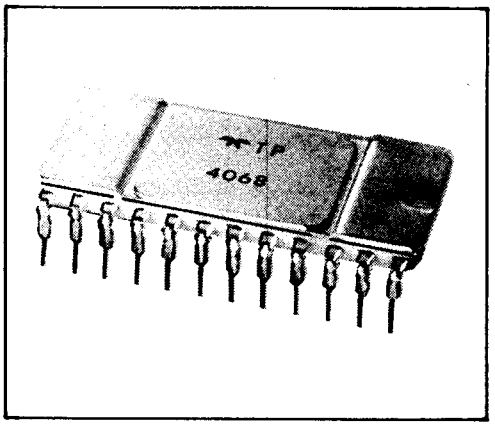


Figure 1. Function Block Diagram



FEATURES

- Monolithic Construction
- Integral and Differential Nonlinearity ± ½LSB Max
- Monotonicity Guaranteed Over Temperature
- 300nsec Settling to ± 0.01%
- Gain Drift ± 10ppm/°C Max. Offset Drift ± 2ppm/°C Max.

APPLICATIONS

- CRT Display Generation
- High Speed A/D Converters
- Video Signal Reconstruction
- Waveform Synthesizers
- Precision Instruments

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SPECIFICATIONS

Each specification is tested at +25°C, V+ = +5 V DC, V– = –15 V DC, V_{ref} = +10 V DC, pin 2 is tied to pin 12, unless otherwise indicated.

	TYPICAL	GUARANTEED
RESOLUTION	---	12 bits
INPUT		
Logic Code		
Unipolar	---	binary
Bipolar	---	offset binary
Switching Levels		
TTL		
"0" State	---	≤0.8 V DC @ –100 μA
"1" State	---	≥2.0 V DC @ 100 nA
CMOS		
"0" State ①	---	≤0.3 V_{ps}+ @ –100μA
"1" State	---	≥0.7 V_{ps}+ @ 100nA
Reference Input	+10 V DC @ 8 kΩ	---
POWER		
V+ ③	5 V DC @ 9 mA	---
V–	–15 V DC @ 28 mA	---
TRANSFER CHARACTERISTICS		
Accuracy ③		
Nonlinearity at 25°C	±¼ LSB	±½ LSB
Nonlinearity, Full Temp. Range	±1 LSB	---
Differential Nonlinearity at 25°C	±¼ LSB	±½ LSB
Differential Nonlinearity, Full Temp. Range	---	monotonic
Zero Offset Error		
Unipolar	---	±0.05% FSR
Bipolar	---	±0.25% FSR
Gain Error	---	±0.25%
Stability		
Zero Offset Error vs. Temp.		
Unipolar	---	±2 ppm of FSR/°C
Bipolar	---	±4 ppm of FSR/°C
Gain Error vs. Temp.	---	±10 ppm/°C
Differential Nonlinearity vs. Temp.	---	±2 ppm of FSR/°C
Power Supply Rejection Ratio		
Unipolar	±0.5 ppm of FSR/%ΔV	---
Bipolar	±1.5 ppm of FSR/%ΔV	---
Gain	---	±3.5 ppm/°C
Dynamic Characteristics		
Settling time, ±½ LSB	300 ns	400 ns
OUTPUT		
Current		
Unipolar	–5 mA	---
Bipolar	±2.5 mA	---
Resistance	1000 Ω	---
Capacitance	20 pF	---
Compliance Voltage	±1 V	---
TEMPERATURE SPECIFICATIONS		
Operating Temperature Range		0°C to 70°C
Storage Temperature Range	---	–65°C to +150°C
ABSOLUTE MAXIMUM RATINGS		
Power Supply Inputs	---	±20 V
Reference Inputs		
V_{ref} (Hi)	---	±V_{ps}
V_{ref} (Lo)	---	0 V
Digital Inputs	---	–1 V to +12 V
Outputs		
Pins 7, 8, 10, 11	---	±V_{ps}
Pin 9	---	+V_{ps}, –5 V
Power Dissipation Package	---	1000 mW

① Pin 1 tied to Pin 2, +4.75 V DC ≤ V+ ≤ +12 V DC.
③ Maximum V+ is 12 V for high level logic, only when pin 1 is tied to pin 2.
③ Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Figure 2.)

APPLICATIONS

Model 4068, a converter with reliability and accuracy, can be used with precision instruments, CRT displays, and data acquisition systems requiring high throughput rates (3.3 MHz) for full range transitions. Because its size will easily fit on a PC board, it is a preferred choice for high speed A/D converter designs and for high speed or high resolution industrial process control systems where space is a limiting factor.

OPERATION

Logic Inputs

Both Models can accept either DTL/TTL or CMOS inputs. If any bits are not to be used, it is recommended that the unused bits be grounded since an "open" bit line is equivalent to a logic "1". Opening the bit lines should not, however, be used as a means of generating a logic "1" due to the possibility of random noise pickup generating an unwanted state.

The 4068 is especially well suited for operation with straight binary, offset binary, or with an inverter on the MSB line two's complement digital inputs. If desired, virtually any other binary code can be used by the addition of the necessary external logic.

Output Range Selection

Desired analog output ranges for pin programming may be found in Table 1. For calibration, use the following procedures.

Bipolar calibration

Step 1: Bipolar Offset – Turn all bits OFF. Adjust R_1 for an output of: –10 V for ±10 V range, –5 V for ±5 V range, and –2.5 V for ±2.5 V range.

Step 2: Gain – Turn bit 1 (MSB) ON; all other bits OFF. Adjust R_2 for zero volts output.

Unipolar calibration

Step 1: Unipolar Offset – Turn all bits OFF. Adjust R_3 for zero volts output.

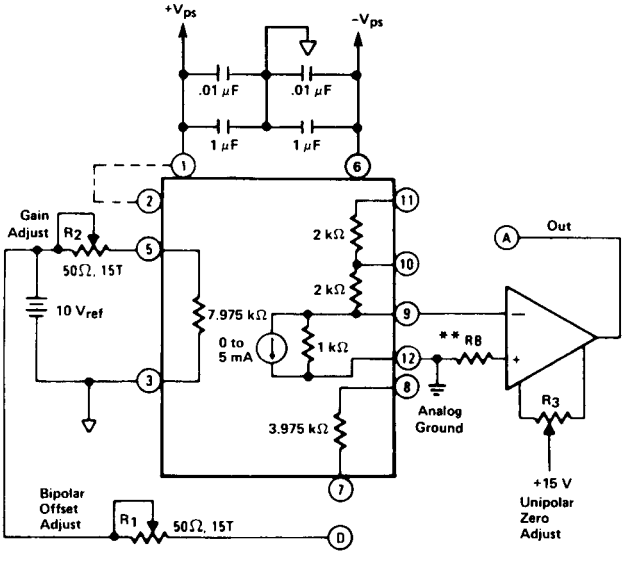
Step 2: Gain – Turn all bits ON. Adjust R_2 for an output of FS –1 LSB. That is, adjust for 9.9976 V for 0 V to +10 V range and 4.9988 V for 0 V to +5 V range.

	OUTPUT RANGE	CONNECTIONS				BIAS (R_B) RESISTOR
		Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	
Unipolar Mode	0 to +10 V	N.C.	N.C.	A	N.C.	667 Ω
	0 to +5 V	N.C.	N.C.	A	9	500 Ω
Bipolar Mode	±10 V	D	9	N.C.	A	667 Ω
	±5 V	D	9	A	N.C.	580 Ω
	±2.5 V	D	9	A	9	444 Ω

Table 1.

Unipolar and Bipolar Voltage Output Connections

Using an external resistive load, the output compliance should not exceed ±1 V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and Table 1.



* **For TTL and DTL compatibility, connect +5 V to pin 1 and ground pin 2. For CMOS compatibility, connect digital power supply (+4.85 V ⩽ VDD ⩽ +12 V) to pin 1 and short pin 2 to pin 1.**

** **Bias resistor (RB) should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current-source output resistance (1 kΩ) and the op amp feedback resistor. See Table 1 for values of RB.**

Figure 2. Trimming and Operation

External Gain and Zero Calibration

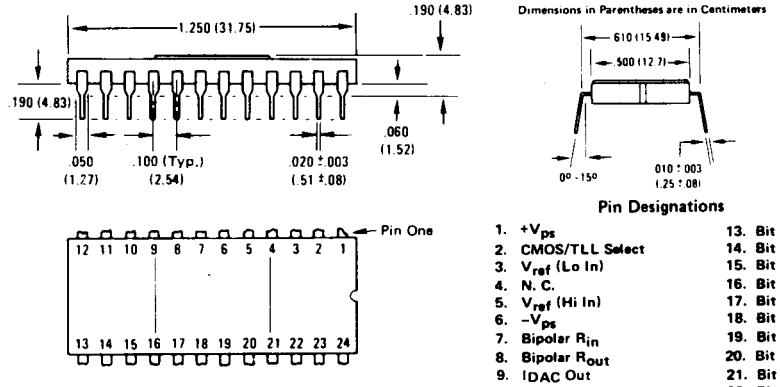
The input reference resistor (7.975 kΩ) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 25 Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the 4068 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient.

Potentiometer R3 conveniently nulls unipolar offset plus op amp offset in one operation. For bipolar-mode operation, R3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 50 Ω potentiometers is ±0.5 LSB and ±0.25 LSB respectively. If desired, the potentiometers can be replaced with fixed 24.9 Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±½ LSB.

Power and Grounding Considerations

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 2 should be used. Decoupling capacitors should be connected close to the unit (preferably to the device pins) and should be tantalum or electroytic bypassed with ceramic types for best high-frequency noise rejection.

Figure 3. Mechanical Specifications



Pin Designations

1. $+V_{ps}$	13. Bit 12 (LSB)
2. CMOS/TLL Select	14. Bit 11
3. V_{ref} (Lo In)	15. Bit 10
4. N. C.	16. Bit 9
5. V_{ref} (Hi In)	17. Bit 8
6. $-V_{ps}$	18. Bit 7
7. Bipolar R_{in}	19. Bit 6
8. Bipolar R_{out}	20. Bit 5
9. IDAC Out	21. Bit 4
10. 10 V Span A	22. Bit 3
11. 20 V Span A	23. Bit 2
12. Ground	24. Bit 1 (MSB)

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