

8, 10, 12 Bit Ultra High Speed A/D Converters

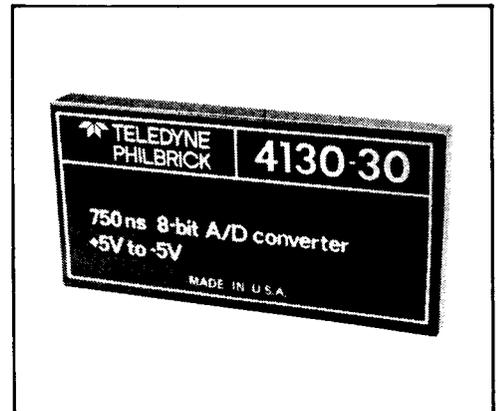
The 4130 Series Ultra High Speed A/D Converters were designed for applications demanding high linearity, excellent stability, fast conversion rates, and guaranteed operation over a wide temperature range. All models use the successive approximation technique for conversion and employ thin-film technology for ultra stable operation. Each converter has its own 10V internal reference and the capability for using an external reference. Digital outputs are fully buffered to eliminate any loading problems that could affect accuracy. Input voltage ranges and conversion times for the various models in the series are summarized below.

MODEL	FULL SCALE INPUT VOLTAGE	MAX CONVERSION TIME	RESOLUTION
4130-10	0 V to -5 V	750 nsec	8 Bits
4130-20	0 V to -10 V		
4130-30	+5 V to -5 V		
4130-40	+10 V to -10 V		
4131-10	0 V to -5 V	1 μ sec	10 Bits
4131-20	0 V to -10 V		
4131-30	+5 V to -5 V		
4131-40	+10 V to -10 V		
4132-22	0 to -10 V, ± 5 V	3.5 μ sec	12 Bits
4133-22	0 to -20 V, ± 10 V (user programmable)	2.5 μ sec	

Applications Information

The single conversion mode is achieved by applying an external pulse to the start convert input. The repetitive conversion mode is achieved by using a TTL inverter as shown in Figure 2. The delay time for the inverter must be added to the total conversion time. Data valid time is shown for both serial and parallel data in Figure 1. Serial output is in a non-return to zero format with the MSB occurring first. The circuit shown in Figure 3 is recommended for storing serial data. The three digital inverters provide approximately 36nsec delay. This delay assures that the information strobed into the shift register is correct because serial data does not become valid until a minimum of 10nsec after each falling clock edge. The circuits shown in Figure 4 are recommended for storing parallel data. The circuit in Figure 4A is recommended for storing data using edge-coupled registers such as an SN74174 or SN74S174. Transfer of information into the registers occurs on the rising edge of the clock pulse. The circuit in Figure 4B is recommended for storing data using DC-coupled registers such as SN7475. Parallel bit information remains valid for a minimum of 20nsec, typically 40nsec, after the rise of the next start convert pulse.

4130 Series



FEATURES

- Fast Conversion Times
 - 750nsec 8 Bits
 - 1 μ sec 10 Bits
 - 2.5 μ sec 12 Bits
- No Missing Codes
- Guaranteed Over Temperature
- Internal Clock and Reference
- Serial and Parallel Output
- Low Drift

APPLICATIONS

- High Speed Data Acquisition
- Fast Fourier Transforms
- Scanning Medical Instrumentation
- Transient Recorders
- Spectrum Analyzers

SPECIFICATIONS At +25°C, ±15 V and +5 V, unless otherwise indicated

MODEL	4130		4131		4132		4133	
	Typical	Guaranteed	Typical	Guaranteed	Typical	Guaranteed	Typical	Guaranteed
RESOLUTION	8 Bit		10 Bit		12 Bit		12 Bit	
INPUTS								
Analog								
Voltage Range/(R _{in})	-5 V/0.5 KΩ ±3 Ω		-5 V/0.5 KΩ ±3 Ω		---		---	
4130-10/4131-10	-10 V/1 KΩ ±5 Ω		-10 V/1 KΩ ±5 Ω		---		---	
4130-20/4131-20	±5 V/1 KΩ ±5 Ω		±5 V/1 KΩ ±5 Ω		---		---	
4130-30/4131-30	±10 V/2 KΩ ±10 Ω		±10 V/2 KΩ ±10 Ω		---		---	
4130-40/4131-40	---		---		±5 V/1 KΩ ± 0.5%		±5 V/1 KΩ ± 0.5%	
4132-22/4133-22	---		---		-10 V/1 KΩ ± 0.5%		-10 V/1 KΩ ± 0.5%	
	---		---		±10 V/2 KΩ ± 0.5%		±10 V/2 KΩ ± 0.5%	
	---		---		-20 V/2 KΩ ± 0.5%		-20 V/2 KΩ ± 0.5%	
Offset Current	±0.4 V/R _{in}							
Reference	---		---		---		---	
Voltage	-10 V		-10 V		-10 V		-10 V	
Resistance	8 KΩ ±0.5%							
Power	+15 V ±0.5 V @ 65 mA max.		+15 V ±0.5 V @ 65 mA max.		+15 V ±0.5 V @ 65 mA max.		+15 V ±0.5 V @ 65 mA max.	
	-15 V ±0.5 V @ 45 mA max.		-15 V ±0.5 V @ 45 mA max.		-15 V ±0.5 V @ 45 mA max.		-15 V ±0.5 V @ 45 mA max.	
	+5 V ±0.25 V @ 325 mA max.		+5 V ±0.25 V @ 325 mA max.		+5 V ±0.25 V @ 325 mA max.		+5 V ±0.25 V @ 325 mA max.	
Recommended Supply	Philbrick 2243		Philbrick 2243		Philbrick 2243		Philbrick 2243	
Digital								
Start Convert	---		---		---		---	
Logic	TTL Positive Pulse							
Conversion Initiation	"0" to "1"							
Pulse Width min./max.	50 to 105 nsec		50 to 130 nsec		50 to 200 nsec		50 to 200 nsec	
Loading ⊙	1 TTL Load							
TRANSFER CHARACTERISTICS								
Accuracy								
Nonlinearity	±½ LSB		±½ LSB		±½ LSB		±½ LSB	
Differential Nonlinearity	±½ LSB		±½ LSB		±½ LSB		±½ LSB	
Quantizing Error	±½ LSB		±½ LSB		±½ LSB		±½ LSB	
No Missing Codes	0 to 70°C							
Monotonicity	0 to 70°C							
Zero Offset Error, (Adj. to Zero)	±25 mV		±10 mV		-11 ±10 mV		-11 ±10 mV	
Unipolar	---		---		-22 ±20 mV		-22 ±20 mV	
Bipolar	±25 mV		±10 mV		-11 ±10 mV		-11 ±10 mV	
Gain Error (Adj. to Zero)	+0.2%		+0.06%		±0.1%		±0.1%	
Stability	---		---		---		---	
Nonlinearity vs. Temp.	±10 ppm/°C		±10 ppm/°C		±5 ppm/°C		±5 ppm/°C	
Differential Nonlinearity vs. Temp.	±5 ppm/°C		±10 ppm/°C		±3 ppm/°C		±3 ppm/°C	
Zero Offset Error vs. Temp.	---		---		---		---	
Unipolar	±15 ppm/°C		±15 ppm/°C		±5 ppm/°C		±5 ppm/°C	
Bipolar	±15 ppm/°C		±15 ppm/°C		±10 ppm/°C		±10 ppm/°C	
Gain Error vs. Temp.	±20 ppm/°C		±20 ppm/°C		±20 ppm/°C		±20 ppm/°C	
Conversion Time vs. Temp.	±0.5 nsec/°C		±1 nsec/°C		±2.8 nsec/°C		±2.8 nsec/°C	
V _{Ref} Out vs. Temp.	±3 ppm/°C		±3 ppm/°C		±3 ppm/°C		±3 ppm/°C	
PSRR	±2.4 mV/V		±2.4 mV/V		±2.4 mV/V		±2.4 mV/V	
Long Term Stability	0.02%/month		0.01%/month		0.007%/month		0.007%/month	
Dynamic Characteristics								
Conversion Time	0.735 μsec		0.980 μsec		3.4 μsec		2.4 μsec	
Conversion Rate	1.333 MHz		1 MHz		0.285 MHz		0.4 MHz	
OUTPUTS								
Reference								
Voltage	-10 V ±1.0%		-10 V ±1.0%		-10 V ±0.1%		---	
Current	-5 mA		-5 mA		-5 mA		-5 mA	
Digital								
Logic Codes	---		---		---		---	
Parallel, Unipolar	BIN		BIN		BIN		BIN	
Parallel, Bipolar	OBIN, 2SC		OBIN, 2SC		OBIN, 2SC		OBIN, 2SC	
Output Drive ⊙	10 TTL Loads							
Serial, Unipolar	BIN		BIN		BIN		BIN	
Serial, Bipolar	OBIN		OBIN		OBIN		OBIN	
Format	NRZ		NRZ		NRZ		NRZ	
Output Drive ⊙	8 TTL Loads							
Switching Levels, all digital outputs								
"0" State	≤ 0.5 V							
"1" State	≥ 2.4 V							
Data Valid Delay ⊙	3 nsec		3 nsec		3 nsec		3 nsec	
Data Valid Margin ⊙	40 nsec		40 nsec		40 nsec		40 nsec	
Status	---		---		---		---	
"1" State	During Conversion		During Conversion		During Conversion		During Conversion	
Output Drive ⊙	4 TTL Loads		5 TTL Loads		4 TTL Loads		4 TTL Loads	
Clock Out								
Logic	TTL Positive Pulse							
Pulse Width	35 nsec		40 nsec		35 nsec		35 nsec	
Rate	13.3 MHz		12.5 MHz		3.8 MHz		5.4 MHz	
Output Drive ⊙	8 TTL Loads							
ENVIRONMENTAL SPECIFICATIONS								
Operating Temp. Range	0 to +70°C							
Storage Temp. Range	-55 to +125°C							
ABSOLUTE MAXIMUM RATINGS								
Supply Voltages to Ground								
±15 V	±18 V		±18 V		±18 V		±18 V	
+5 V	+6 V		+6 V		+6 V		+6 V	
Digital Input Voltage	+5 V		+5 V		+5 V		+5 V	
Analog Input Voltage								
R _{in} = 500 Ω	±11 V		±11 V		±11 V		±11 V	
R _{in} = 1000 Ω	±16 V		±16 V		±16 V		±16 V	
R _{in} = 2000 Ω	±22 V		±22 V		±22 V		±22 V	

⊙ A Standard TTL unit load is -1.6 mA at +0.4 V (LO) and +40 μA max. at +2.4 V (HI).
 ⊙ Delay from fall of Status Signal before LSB becomes valid.
 ⊙ Minimum time data from previous conversion is valid after rise of next start convert pulse.

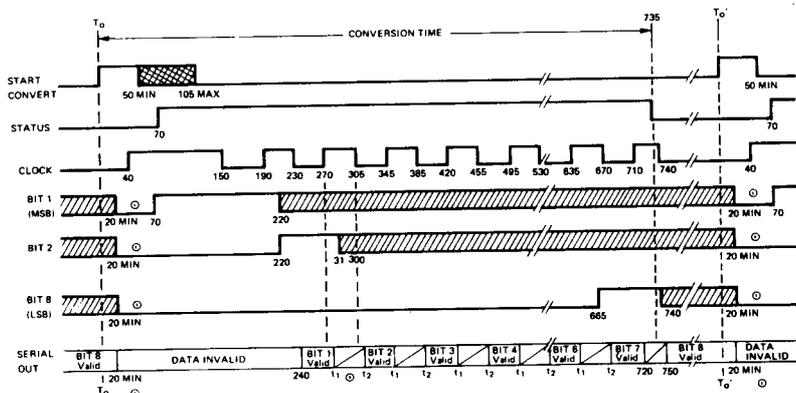


Figure 1A. Model 4130 Timing Diagram

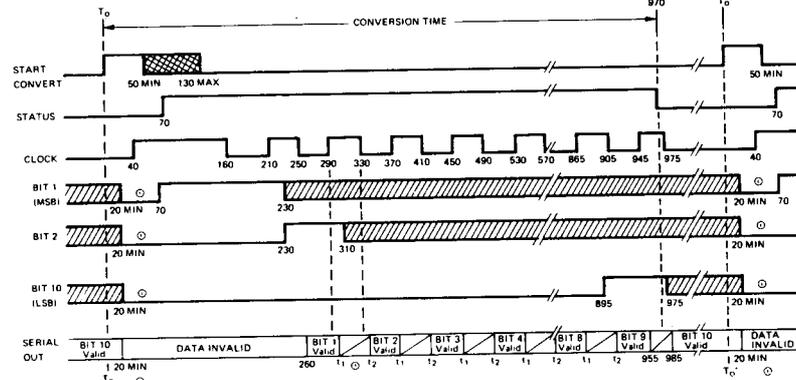


Figure 1B. Model 4131 Timing Diagram

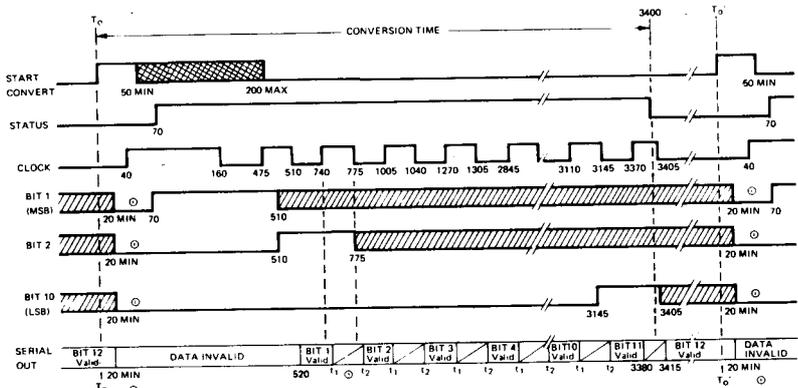
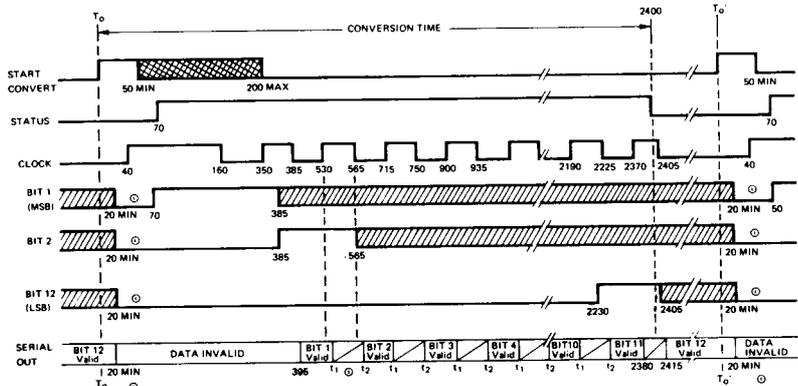


Figure 1C. Model 4132 Timing Diagram



⊙ DATA VALID MINIMUM OF 20 NSEC AFTER RISE ON START CONVERT PULSE
 ⊙ ALL TIMES ARE EXPRESSED IN NSEC AND ARE RELATIVE TO T_0 TO OR T_0'
 // PARALLEL DATA VALID
 ⊙ SERIAL DATA IS INVALID BETWEEN TIMES t_1 AND t_2 WHERE t_1 OCCURS 10 NSEC MAX AFTER THE RISE ON THE CLOCK PULSE AND t_2 OCCURS 10 NSEC MIN AFTER THE FALL ON THE CLOCK PULSE.

Figure 1D. Model 4133 Timing Diagram

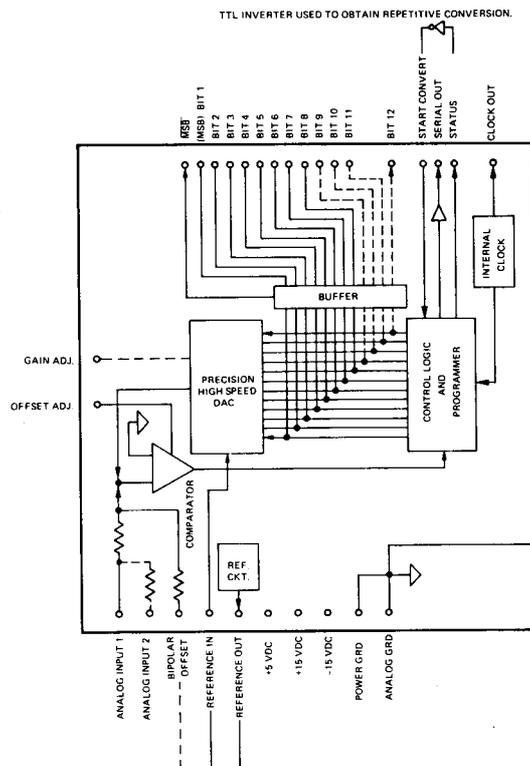
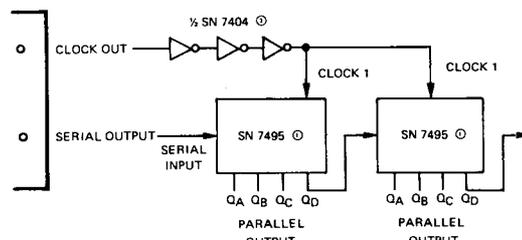
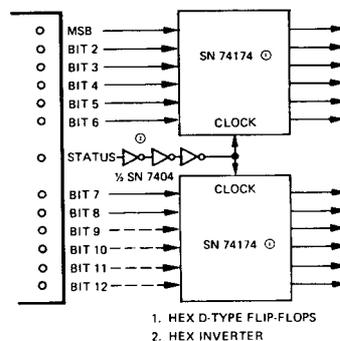


Figure 2. Functional Block Diagram



NOTES: 1. 4 BIT PARALLEL-ACCESS SHIFT REGISTERS
 2. HEX INVERTER

Figure 3. Storing Serial Data



1. HEX D-TYPE FLIP-FLOPS
 2. HEX INVERTER

Figure 4A. Edge Coupled Registers

4130 Series

OFFSET TRIMMING

1. Unipolar Mode

Apply $-1/2$ LSB of voltage to the Analog Input and adjust the Offset Trim potentiometer, see Figure 5, for a digital output which is exactly on the threshold of changing from all 0's to 000...001.

2. Bipolar Mode

Apply $+F.S. -1/2$ LSB of voltage to the Analog Input and adjust the Offset Trim potentiometer, see Figure 5, for an output which is exactly on the threshold of changing from all 0's to 000...001.

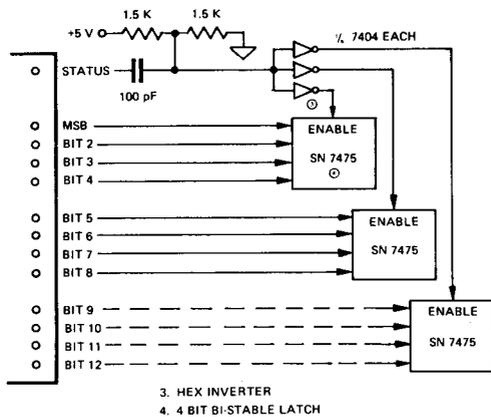


Figure 4B. DC Coupled Registers

Analog Input	UNIPOLAR	BIPOLAR	
	Binary	Offset Binary	2's Complement
+ FS	000 ... 000	000 ... 000	100 ... 000
+ FS - 1 LSB	000 ... 001	000 ... 001	100 ... 001
+ 3/4 Scale	001 ... 000	001 ... 000	101 ... 000
+ 1/2 Scale	010 ... 000	010 ... 000	110 ... 000
0 + 1 LSB	011 ... 111	011 ... 111	111 ... 111
0	000 ... 000	100 ... 000	000 ... 000
0 - 1 LSB	000 ... 001	100 ... 001	000 ... 001
- 1/2 Scale	100 ... 000	110 ... 000	010 ... 000
- 3/4 Scale	110 ... 000	111 ... 000	011 ... 000
- FS + 1 LSB	111 ... 111	111 ... 111	011 ... 111

Figure 6. Digital Code Table

POWER AND GROUNDING CONSIDERATIONS

High speed systems require added care in power distribution for maximum accuracy and speed. Although power supply inputs on all models are internally bypassed, it is recommended that a $1 \mu F$ tantalum capacitor and a $0.01 \mu F$ disc capacitor be added externally to each supply input for optimum performance.

The Analog Ground and Power Ground are internally connected on Models 4130 and 4131. Therefore, the system power ground must be very low impedance to ensure that there are no ground loop errors. All models are housed in a metal case which is internally connected to Power Ground.

GAIN TRIMMING

Apply $-F.S. + 3/2$ LSB of voltage to Analog Input and adjust the Gain Trim potentiometer, see Figure 5, for a digital output which is exactly on the threshold of changing from 111...110 to 111...111.

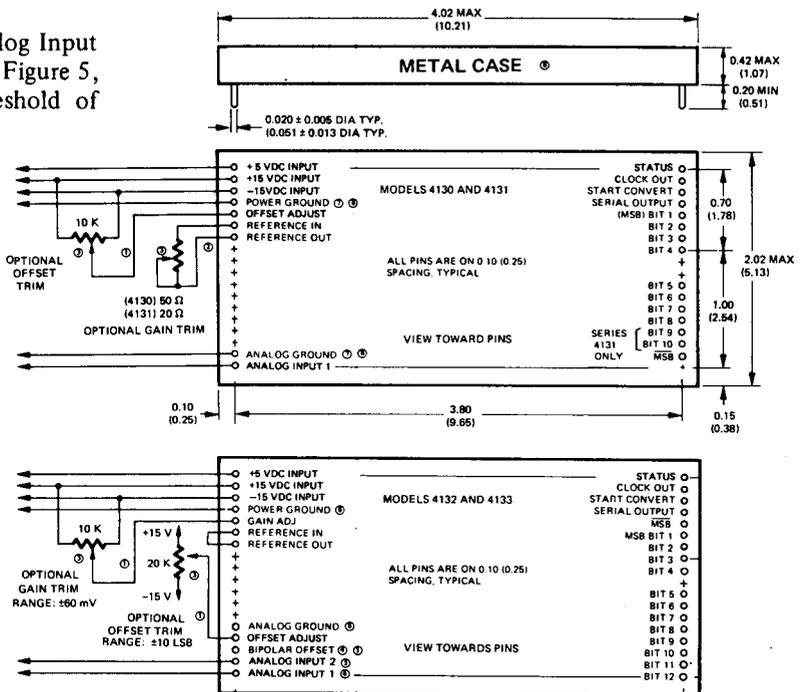


Figure 5. Mechanical Dimensions and Optional Trim Circuits

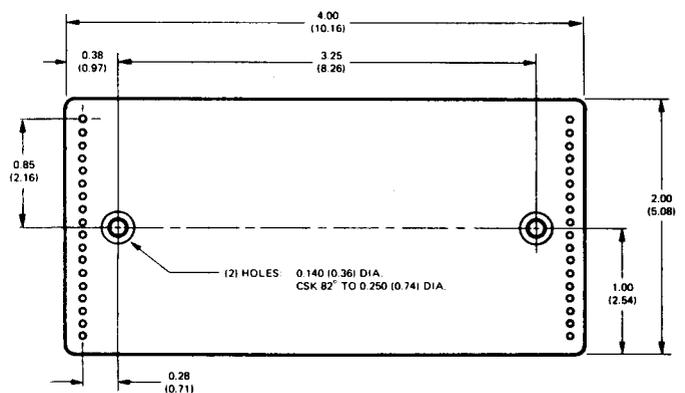


Figure 7. Optional Socket Model 6132

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