⊤⊤ TELEDYNE PHILBRICK

2μsec, 12 Bit Progressive Approximation Analog to Digital Converter

4134

The 4134 is a 12 bit A/D converter that uses the new progressive approximation A/D conversion technique. The 4134's internal clock employs a sense and accelerate circuit that increases its frequency after bit 4 has been determined. This technique is based on the fact that it takes a successive approximation A/D converter longer to make decisions on higher order bits than it does on lower order bits, and it enables the 4134 to make a complete 12 bit conversion in 2μsec maximum. The 4134 has 4 input ranges, an internal reference, and an output buffer to eliminate loading problems.

Applications Information

Conversion is achieved by applying a positive going pulse to the start convert input. The repetitive conversion mode is achieved by using a TTL inverter, as shown in Figure 1. For applications requiring greater accuracy, use the following offset and gain trimming procedures. For unipolar offset, apply − 1/2LSB of voltage, and adjust the offset potentiometer so the digital output just changes from all 0's to 000...001. For bipolar offset, apply + FS − 1/2LSB of voltage, and adjust the offset potentiometer so the digital output just changes from all 0's to 000...001. For gain, apply − FS + 3/2LSB of voltage, and adjust the gain potentiometer so the digital output just changes from all 1's to 111...110. For optimum performance, all power supplies should be bypassed with 1μF tantalum and 0.01μF ceramic capacitors.

Figure 1. Functional Block Diagram

FEATURES

- 2μsec Maximum Conversion Time
- Progressive Approximation A/D Conversion Technique
- No Missing Codes Over Temperature
- ± 1/2LSB Integral and Differential Nonlinearities
- Serial and Parallel Outputs

APPLICATIONS

- High Speed DAS's
- Fast Fourier Transforms
- Scanning Medical Instrumentation
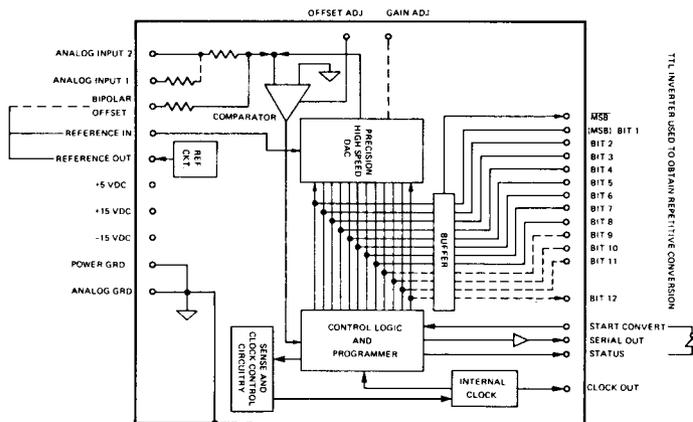- Transient Recorders
- Radar Signal Processing

SPECIFICATIONS (T_A = +25°C, ±15 V and +5 V supplies unless otherwise indicated).

	TYPICAL	GUARANTEED
RESOLUTION		12-Bit
INPUTS		
Analog	---	±5 V/1 kΩ ±0.5%
	---	−10 V/1 kΩ ±0.5%
	---	±10 V/2 kΩ ±0.5%
	---	−20 V/2 kΩ ±0.5%
Offset Current	±0.4 V/R_{in}	
Reference		
Voltage	−10 V	---
Resistance	---	8 kΩ ±0.5%
Power	---	+15 V ±0.5 V @ 65 mA max.
	---	−15 V ±0.5 V @ 45 mA max.
	---	+5 V ±0 25 V @ 325 mA max.
Recommended Supply	Philbrick 2243	
Digital		
Start Convert		
Logic		TTL Positive Pulse
Conversion Initiation	---	"0" to "1"
Pulse Width min./max.	---	75 to 200 ns
Loading	---	1 TTL Load
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity	±½ LSB	±1 LSB
Differential Nonlinearity	±½ LSB	---
No Missing Codes	---	0°C to +50°C
Monotonicity	---	0°C to +70°C
Zero Offset Error		
(Adj. to zero)		
Unipolar	---	±20 mV
Bipolar	---	±20 mV
Gain Error (Adj. to zero)	---	±0.1%
Stability		
Nonlinearity vs Temp.	---	±5 ppm/°C
Differential Nonlinearity	±3 ppm/°C	±5 ppm/°C
Zero Offset Error vs Temp.		
Unipolar	---	±5 ppm/°C
Bipolar	---	±10 ppm/°C
Gain Error vs Temp.	---	±20 ppm/°C
Conversion Time vs Temp.	---	±2.8 ns/°C
V_{ref} Out vs Temp.	±3 ppm/°C	±10 ppm/°C
PSRR	±2.4 mV/V	---
Long Term Stability	0.007%/Month	---
Dynamic Characteristics		
Conversion Time	1.8 µs	2.0 µs
Conversion Rate	---	0.5 MHz
OUTPUTS		
Reference		
Voltage	---	−10 V ±0.1%
Current	−5 mA	---
Digital		
Logic Codes		
Parallel, Unipolar	BIN	
Parallel, Bipolar	OBIN, 2SC	
Output Drive ①	---	10 TTL Loads
Serial, Unipolar	BIN	
Serial, Bipolar	OBIN	
Format	NRZ	
Output Drive ①	---	8 TTL Loads
Switching Levels,		
all digital outputs		
"0" State	---	⩽0.5 V
"1" State	---	⩾2.4 V
Data Valid Delay ②	3 ns	10 ns
Data Valid Margin ③	40 ns	20 ns
Status		
"1" State	During Conversion	
Output Drive ①	---	4 TTL Loads
Clock Out		
Logic		TTL Positive Pulse
Pulse Width	35 ns	---
Rate	3.5 MHz to 7.6 MHz	---
Output Drive ①	---	8 TTL Loads
ENVIRONMENTAL SPECIFICATIONS		
Operating Temp. Range	---	0°C to +70°C
Storage Temp. Range	---	−25°C to +85°C
ABSOLUTE MAXIMUM RATINGS		
Supply Voltages to Ground		
±15 V	---	±18 V
+5 V	---	+6 V
Digital Input Voltage	---	+5 V
Analog Input Voltage		
R_{in} = 500Ω	---	±11 V
R_{in} = 1000Ω	---	±16 V
R_{in} = 2000Ω	---	±22 V
RECOMMENDED SOCKET	Model 6132	

① A standard TTL unit load is −1.6 mA at +0.4 V (LO) and +40 uA max. at +2.4 V (HI).
② Delay from fall of status signal before LSB becomes valid.
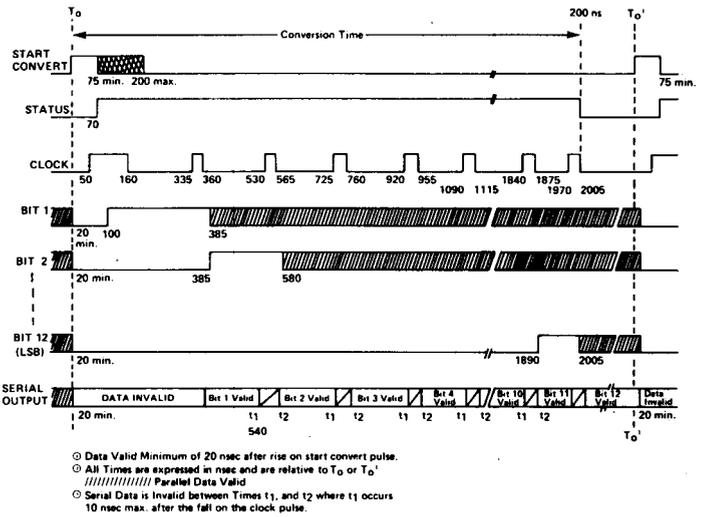③ Minimum time data from previous conversion is valid after rise of next start convert pulse.

① Data Valid Minimum of 20 nsec after rise on start convert pulse.
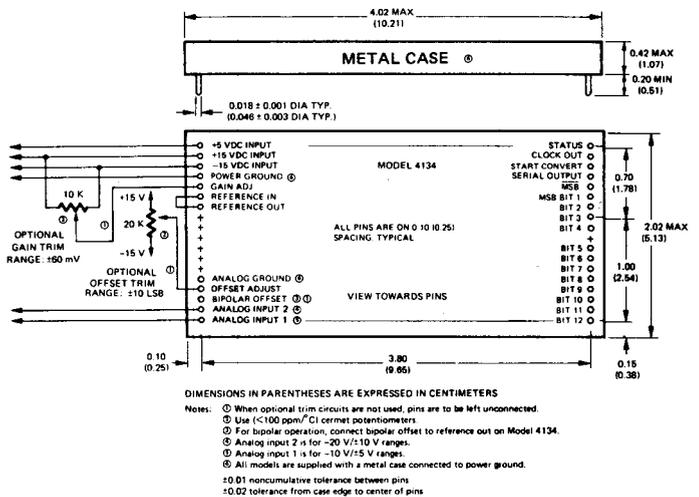② All Times are expressed in nsec and are relative to T_0 or T_0'
/////////////// Parallel Data Valid
③ Serial Data is Invalid between Times t_1 and t_2 where t_1 occurs
10 nsec max. after the fall on the clock pulse.

Figure 2. Model 4134 Timing Diagram

DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS
Notes: ① When optional trim circuits are not used, pins are to be left unconnected.
② Use (<100 ppm/°C) cermet potentiometers.
③ For bipolar operation, connect bipolar offset to reference out on Model 4134.
④ Analog input 2 is for −20 V/±10 V ranges.
⑤ Analog input 1 is for −10 V/±5 V ranges.
⑥ All models are supplied with a metal case connected to power ground.
±0.01 noncumulative tolerance between pins
±0.02 tolerance from case edge to center of pins

Figure 3. Mechanical Dimensions

	UNIPOLAR	BIPOLAR	
Analog Input	**Binary**	**Offset Binary**	**2's Complement**
+ FS		000 . . . 000	100 . . . 000
+ FS − 1 LSB		000 . . . 001	100 . . . 001
+³/₄ Scale		001 . . . 000	101 . . . 000
+ ½ Scale		010 . . . 000	110 . . . 000
0 + 1 LSB		011 . . . 111	111 . . . 111
0	000 . . . 000	100 . . . 000	000 . . . 000
0 − 1 LSB	000 . . . 001	100 . . . 001	000 . . . 001
− ½ Scale	100 . . . 000	110 . . . 000	010 . . . 000
− ³/₄ Scale	110 . . . 000	111 . . . 000	011 . . . 000
− FS + 1 LSB	111 . . . 111	111 . . . 111	011 . . . 111

Figure 4. Digital Code Table