TELEDYNE PHILBRICK

8, 10, 12 Bit CMOS A/D Converters with Tri-State Outputs

4143
4144
4145

The 4143/4144/4145 are 8/10/12 bit monolithic CMOS analog-to-digital converters, respectively, with Tri-State outputs. These devices are fully self-contained in single 24 pin dual-in-line packages that require only a few passive support components for operation. Fully specified performance is guaranteed over each device's entire operating temperature range.

A/D conversion is accomplished using an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of an unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion, the total count is latched into the digital outputs as an 8/10/12 bit binary word. Maximum integral and differential nonlinearities of ± ½LSB, typical power dissipation of 20mW, monotonic performance over the entire operating temperature range, and good temperature stability are only a few of the inherent characteristics of these monolithic devices.

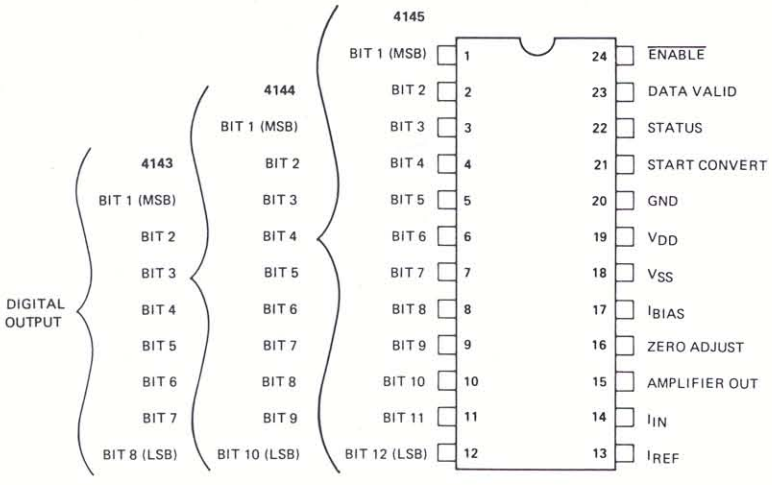
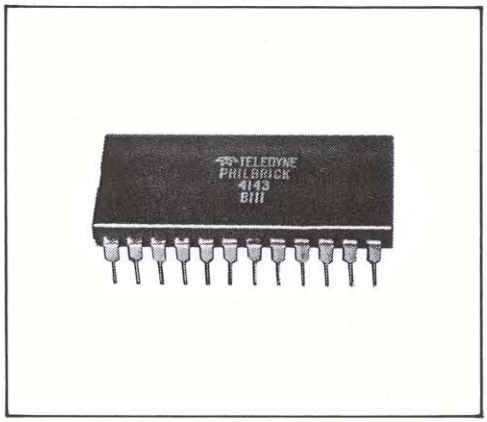


Figure 1. Pin Designations



FEATURES

- Low Power Dissipation
- Monolithic 24 Pin DIP Package
- No Missing Codes Over Temperature
- High Temperature Stability
- Binary Tri-State Outputs
- CMOS, TTL (Low-Power & LS) Compatible

APPLICATIONS

- Data Acquisition
- Process Control
- Portable Measuring Equipment
- Low Cost Microprocessor Based Data Acquisition
- Tracking A/D Conversion

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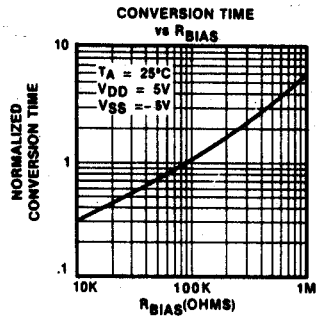
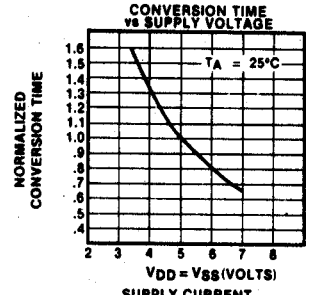
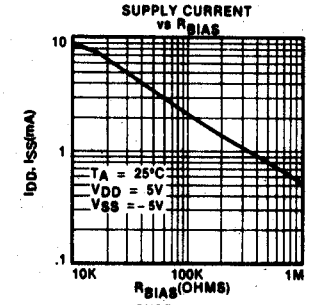
SPECIFICATIONS At 25°C with V_{DD} = +5 V, V_{SS} = −5 V, V_{GND} = 0 V, V_{REF} = −6.4 V, and R_{BIAS} = 100 KΩ, unless otherwise specified.

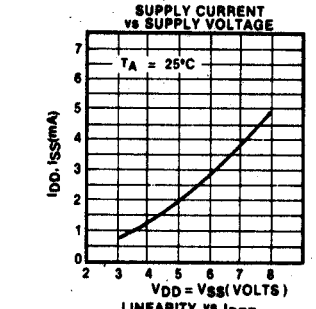
	TYPICAL	GUARANTEED
RESOLUTION		
4143	---	8-bits
4144	---	10-bits
4145	---	12-bits
INPUTS		
Analog		
I_{IN} Full Scale ①	10 μA	---
I_{REF} ①	−20 μA	---
Power		
I_{DD} Quiescent	1.4 mA	2.5 mA
I_{SS} Quiescent	−1.6 mA	−2.5 mA
V_{DD} & V_{SS} Operating Range	±3 V to ±7 V	---
Digital		
Start Convert		
Logic	CMOS or TTL (Low-Power & LS)	
Conversion Initiation	---	"0" to "1"
Pulse Width, min.	---	500 nsec
Loading	---	1 CMOS Load
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity	---	±½ LSB
Differential Nonlinearity	±¼ LSB	±½ LSB
Zero Offset (Adj. to Zero)	±10 mV	±50 mV
Gain Error (Adj. to Zero)	±2%	±5%
Stability		
(Diff.) Nonlinearity vs. Temp.	±2.5 ppm/°C	±5 ppm/°C
Zero Offset vs. Temp.	±30 μV/°C	±50 μV/°C
Gain Error vs. Temp.	±25 ppm/°C	±75 ppm/°C
PSRR, V_{DD} & V_{SS} = ±1 V	±0.5%/V	±1.0%/V
PSRR, V_{DD} & V_{SS} = ±1 V (Tracking)	±0.05%/V	±0.1%/V
Dynamic		
Conversion Time 4143	1.25 msec	1.8 msec
4144	5.0 msec	6.0 msec
4145	20.0 msec	24.0 msec
CONVERSION TIME IN FREE RUN MODE		
4143	1.25 msec	---
4144	5.0 msec	---
4145	20.0 msec	---
OUTPUTS		
Digital		
Logic Codes		
Parallel, Unipolar	BIN	
Parallel, Bipolar ②	OBIN	
Output Drive	---	5 LP TTL Loads
Switching Levels, all digital outputs ③		
"0" State	---	≤.4 V
"1" State	---	≥2.4 V
Data Valid, "1" state for valid data	5 μsec	---
Busy		
"1" State	During Conversion	
Output Drive	---	5 LP TTL Loads
Enable Propagation Delay	500 nsec	1 μsec
ENVIRONMENTAL SPECIFICATIONS		
Operating Temp. Range 4143/4144/4145	---	0°C to +70°C
Storage Temp. Range	---	−65°C to +150°C
ABSOLUTE MAXIMUM RATINGS		
V_{DD} − V_{SS}	---	18 V
I_{IN}	---	±10 mA
I_{REF}	---	±10 mA
Digital Input Voltage	---	−0.3 V to V_{DD} +0.3 V
Package Dissipation	---	500 mW
Lead Temperature (10 seconds)	---	300°C

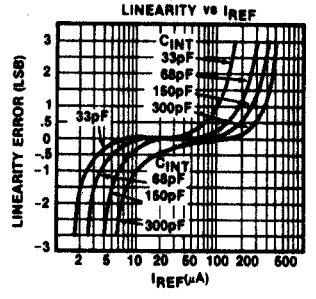
① This pin is connected to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Figure 2.
② Bipolar operation can be obtained by offsetting the input at pin14. Care should be taken not to exceed the 10 μA full scale current.
③ Unused pins of 4143 & 4144 are internally connected to ground.











HANDLING PRECAUTIONS

The 4143/4144/4145 series are CMOS devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

APPLICATIONS

Input/Output Relationships – The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{DIGITAL COUNTS} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 4143
A = 2064 for 4144
A = 8208 for 4145

where DIGITAL COUNTS is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

ANALOG INPUT	DIGITAL MSB LSB
$V_{IN} \geq$ Full Scale	1 . . . 1 1 1 . . . 1
= Full Scale 1 LSB	1 . . . 1 1 1 . . . 1
= 1 LSB	0 . . . 0 0 0 . . . 1
≤ 0	0 . . . 0 0 0 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection – Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{REF} – Values of these components are chosen to give a full scale input current of approximately 10 μA and a reference current of approximately –20 μA.

Examples:

$$R_{IN} \cong \frac{V_{IN\ FULL\ SCALE}}{10\,\mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\,\mu A}$$

$$R_{IN} \cong \frac{10\ V}{10\,\mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\,\mu A} = 320\ K\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using an optional gain adjust circuit to obtain full scale output at $V_{IN\ FULL\ SCALE}$ (see adjustment procedure.) Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS} – Specifications for the 4143/4144/4145 are based on R_{BIAS} = 100 KΩ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 K the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 MΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA.)

R_{DAMP} – Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP} – Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT} – Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF} – A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

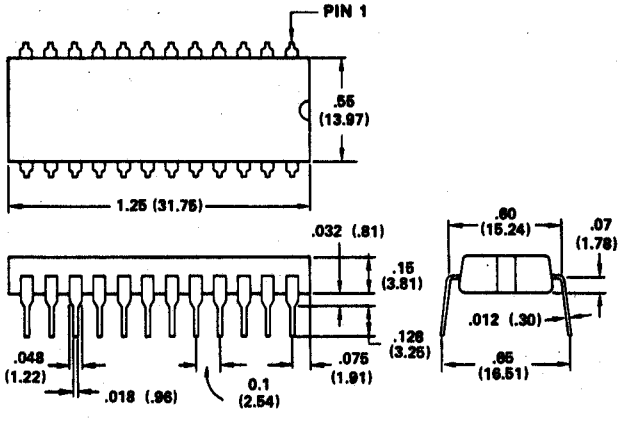
V_{DD}, V_{SS} – Power supplies of ±5 V are recommended, with 0.1 μF decoupling capacitors.

Adjustment Procedure – The test circuit diagram shows optional circuits for trimming the zero location and full scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full scale), it is recommended that transition points be used in setting the zero and full scale values. Recommended procedure is as follows:

1. Set the start convert control high to provide free-run operation and verify that converter is operating.
2. Set V_{IN} to +½ LSB and trim the zero adjust circuit to obtain a 000 . . . 000 to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1½ LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

PHYSICAL DIMENSIONS



All dimensions are typical values unless stated otherwise. Dimensions in parentheses are expressed in millimeters.

24-Pin Plastic DIP

Figure 2. Functional Block Diagram

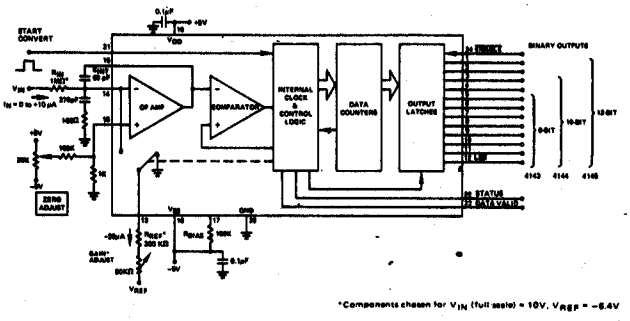
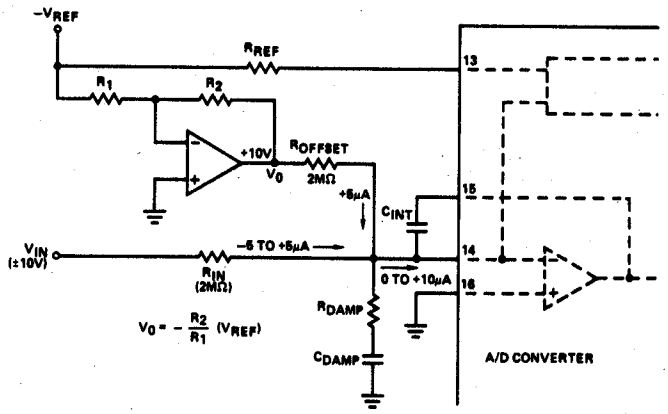


Figure 3. Offset Binary



Two's complement coding may be generated by inverting the MSB output.

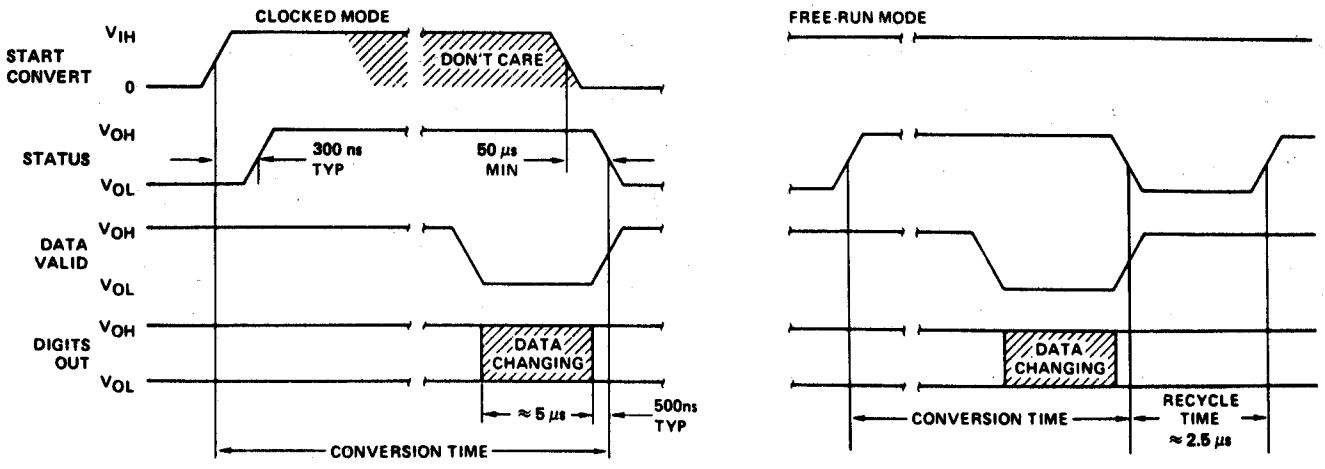
CIRCUIT DESCRIPTION

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is proportional to the reference voltage and is of opposite sign to I_{IN}. I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end of conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Start Convert input is strobed with a positive signal, the Status line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Status is true high, and when the circuit is converting, Start Convert has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Figure 4. Timing Diagram (Rise, fall times = 200 ns typ., C_L = 50 pF)



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