TELEDYNE PHILBRICK

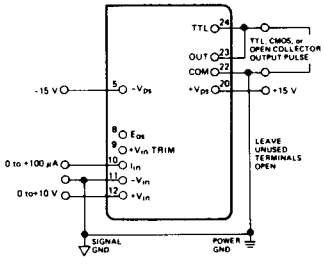
10kHz, 100kHz, 1MHz High Reliability, Differential Voltage to Frequency Converters

4731
4733
4735

The 4731, 4733, and 4735 are precision, low drift voltage to frequency converters that are capable of producing 10kHz, 100kHz, and 1MHz output pulse trains from ± 10μV to ± 10V input signals. With 126dB dynamic range, 70dB CMRR, and 100% overrange, these devices have the ability to handle both voltage and current input signals. The current pin (the summing point of an op amp) resolves currents as low as 1000pA (4731/4733), allowing operation with full scale input voltages from less than 250mV to greater than 100 volts. The 4731/4733's ±0.002%FS nonlinearity is the equivalent of 16 bit end point linearity, while differential nonlinearity and dynamic range approach 20 bits. Housed in a 24 pin ceramic package, standard devices are specified over the 0 to +70°C temperature range. For maximum reliability and performance, these devices are available screened to MIL-STD-883B (add -83 to part number) and specified over the −55°C to +125°C temperature range. Applications include high common mode voltage isolation, digital data transmission and high resolution analog to digital converters.

Applications Information

When used as shown in Figures 1A & 1B, the factory trimmed V/F operates as specified without additional components. Pin 9 (+V_{in} trim) and pin 12 (+V_{in}) are both inputs for a positive input signal. Pin 12 can be used when accuracy to ±0.1% of FS is needed with no external components. Pin 9 is usually used when greater accuracy is required using an external trim, see Figure 2A.



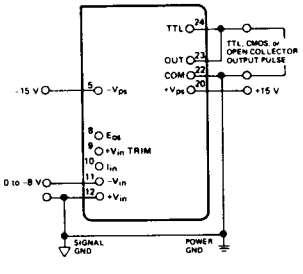
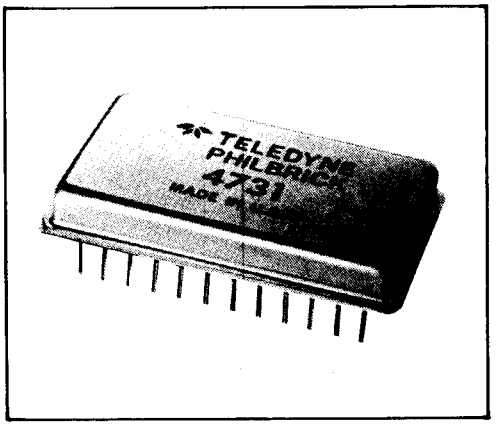


Figure 1A. Positive Input Signals **Figure 1B. Negative Input Signals**



FEATURES

- ±0.005%FS Max Nonlinearity
- 100% Overrange
- 126dB Dynamic Range
- 70dB CMRR
- Low Full Scale and Zero Offset Voltage Drift

APPLICATIONS

- No Drift Integrate/Hold
- High Common Mode Voltage Isolation
- 2 Wire Digital Transmission
- Analog to Digital Converters
- Optical Data Link

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SPECIFICATIONS @ +25°C, ±V_{cc}, ±15 V (unless otherwise indicated)

	TYPICAL	GUARANTEED
FULL SCALE (FS)		
Ideal Transfer Function	---	$f_{out} = \frac{(V_{in})(f_A)}{10\ V} = \frac{(I_{in})(f_A)}{I_{fs}}$ ⑦
f_A		10 kHz (4731)/100 kHz (4733)/1 MHz (4735)
$+V_{in}$ trim	---	9.9 V ±0.5% trimmable to 10.00 V
$+V_{in}$	---	10.00 V ±.05 V
$+I_{in}$	---	100 µA ±25% (4731/4733); 1 mA ±25% (4735)
Range (for specified nonlinearity) ①		
$+V_{in}$ Terminal	+10 µV to +21 V	+100 µV to +12 V
$-V_{in}$ Terminal @ V_{cc} = ±18 V	−10 µV to ($-V_{cc}$ +5.0 V)	−100 µV to ($-V_{cc}$ +7.0 V)
$+I_{in}$ Terminal	+1 nA to +210 µA (4731/4733)	+1 nA to 120 µA (±25%) (4731/4733)
	10 nA to +2.1 mA (4735)	10 nA to 1.2 mA (4735)
Differential $[(+V_{in}) - (-V_{in})]$ ③	±12 V	±11 V, ($\pm V_{cc}$ fault)
Over Range Max., $+V_{in}$, ($-V_{in}$ = 0)	$+V_{in}$ = 21 V, f_{out} = 21 kHz/210 kHz/2.1 MHz	$+V_{in}$ = +20 V, f_{out} = 20 kHz/200 kHz (4731/4733); $+V_{in}$ = +15 V, f_{out} = 1.5 MHz (4735)
Dynamic Range	126 dB	100 dB
Common Mode Voltage ②	($+V_{cc}$ −4 V), ($-V_{cc}$ +5 V)	($+V_{cc}$ −5 V), ($-V_{cc}$ +7 V)
CMRR, CMV = ±10 V	70 dB	60 dB

NONLINEARITY ±%FS	**4731/4733**	**4735**	**4731/4733**	**4735**
$+V_{in}$ (+100 µV to 12 V)	.002	.005	.005	.015
$+V_{in}$ (+100 µV to 12.0 V) ④⑧	.002	.005	.005	.015
$-V_{in}$ (−100 µV to $-V_{cc}$ +7.0 V)	.01	.02	.02	.05
$+I_{in}$ (1 nA to 120 µA) (4731/4733)	.002	---	.005	---
$+I_{in}$ (1 nA to 120 µA) (4731/4733) ④⑧	.002	---	.005	---
$+I_{in}$ (10 nA to 1.2 mA) (4735)	---	.005	---	.015
$+I_{in}$ (10 nA to 1.2 mA) (4735) ④⑧	---	.005	---	.015
$+V_{in}$ (+100 µV to +12.0 V) ⑥	.005	.01	.01 Hot; .03 Cold	.02
$+V_{in}$ (+100 µV to 20 V) (4731/4733) ④⑧	.02	---	.05	---
$+V_{in}$ (+100 µV to 15 V) (4735) ④⑧	---	.02	---	.05

INPUT		
Zero Offset Voltage, Initial Untrimmed	±1 mV	±5 mV (trimmable to zero)
Impedance @ $+V_{in}$	---	100 kΩ±25% (4731/4733); 10 kΩ±25% (4735)
Impedance @ $-V_{in}$	100 MΩ	10 MΩ
Impedance @ $+I_{in}$ (op amp summing point)	Virtual Ground	< 0.1 Ω

STABILITY OF FULL SCALE FACTOR	**4731**		**4733**		**4735**	**4731**		**4733**		**4735**
	Hot	Cold	Hot	Cold	⑧	Hot	Cold	Hot	Cold	⑧
Temperature Coefficient ($+V_{in}$, $-V_{in}$) ±PPM/°C ④	4	7	6	10	30	15	25	20	30	50
Temperature Coefficient ($+I_{in}$) ±PPM/°C ④	4	7	6	10	30	---	---	---	---	---
Temperature Coefficient ($+V_{in}$, $-V_{in}$) ±PPM/°C ⑥	8	10	12	15	30	25	50	30	50	50
Power Supply Sensitivity ±PPM/%ΔV_{cc} ③	10		10		15	20		20		35
Drift: Per Day/Per Month ±PPM	10/30		10/30		10/30	---		---		---
Warm Up Time to .01%/.002% of F.S.	1 s/100 s		1 s/100 s		1 s/100 s	---		---		---

STABILITY OF ZERO OFFSET VOLTAGE µV/°C	**4731/4733**	**4735**	**4731/4733**	**4735**
Temperature Coefficient µV/°C ④	±6	±10	±20	±50
Temperature Coefficient µV/°C ⑥	±20	±15	±100 Hot; ±50 Cold	±50
Power Supply Sensitivity ±µV/%ΔV_{cc} ③	3	5	20	10
Drift: Per Day/Per Month	20 µV/60 µV	20 µV/60 µV	---	---

RESPONSE		
Settling Time to .01% for FS step input	---	1 to 2 pulses of new frequency +5 µs
Overload Recovery (V_{in} = +100 V to V_{in} = +10) or (I_{in} = 1 mA to I_{in} = 100 µA)	0.14 ms (4731/4733); 70 µs (4735)	0.5 ms (4731/4733); 0.2 ms (4735)

OUTPUT WAVEFORM		TTL compatible
High (positive logic "1")	---	+2.4 V to +5 V (up to 10 TTL Load)
Low (positive logic "0")	---	≤ 0.4 V @ −16 mA Sink Current
Pulse Width	---	(4731/10 µs to 30 µs, 4733/1 µs to 3 µs, 4735/0.1 µs to .3 µs)
Source Impedance (High)	---	3.5 kΩ±20% (4731/4733); 680 Ω±20% (4735)

POWER REQUIREMENT		
Voltage Range ($\pm V_{cc}$)	±7 V to ±18 V	±9 V to ±18 V
Voltage Asymmetry (Δ between $\lvert+V_{cc}\rvert$ & $\lvert-V_{cc}\rvert$	---	±2 V
Current ($\pm I_{cc}$) @ V_{cc} = ±15 V	±17 mA (4731/4733); ±35 mA (4735)	±25 mA (4731/4733); 45 mA (4735)

ENVIRONMENT/RELIABILITY		
Operating Temperature	---	0°C to +70°C
-83		−55°C to +125°C
Storage Temperature Absolute Max.	---	−65°C to +150°C

Input Protection: All inputs may be shorted to ±V_{cc} indefinitely without damage

Output Protection: May be shorted to ground indefinitely; to +V_{cc} for 5 s

NOTES

① After trim @ 10 Hz and 10 kHz (4731)/100 Hz and 100 kHz (4733)/1 kHz and 1 MHz (4735)
② See Figure 5G for definition
③ Constant voltage at Zero trim pin
④ Measured from −25°C to +85°C, Hot (+25°C to +85°C) & Cold (−25°C to +25°C)
⑤ Measurement, made for ±V_{cc} = ±9 V to ±18 V
⑥ Measured for −55°C to +125°C, Hot (+25°C to +125°C) & Cold (−55°C to +25°C)
⑦ I_{fs} = 100 µA for 4731 and 4733, 1 mA for 4735
⑧ Specified over entire temperature range, −55°C to +125°C

Zero & Full Scale Trim

When greater accuracy is required, input offset voltage (E_{OS}) is trimmed to ZERO and Full Scale (FS) output frequency f_{out} is trimmed to 10.00 kHz/100.0 kHz/1 MHz with external potentiometers as illustrated in Figure 2. (Note: Full Scale trim components should have temperature coefficients similar to Full Scale TC of the V-to-F being used).

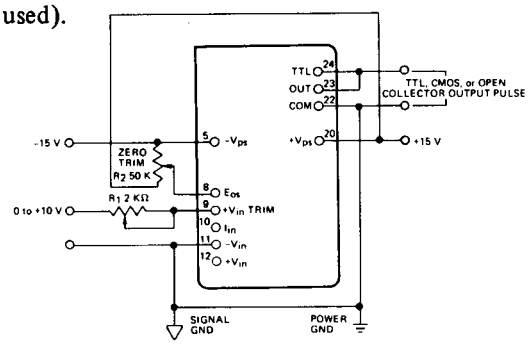


Figure 2A. Positive Voltage Input

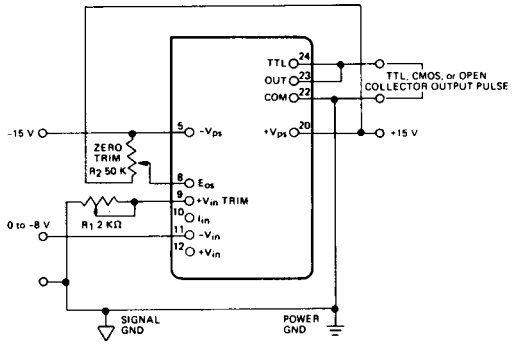


Figure 2B. Negative Voltage Input

TRIM PROCEDURE

1. Apply 10 mV between the + voltage input terminal and ground; then adjust R2 for f_{out} = 10 Hz on the 4731, 100 Hz on the 4733 and 1 kHz on the 4735.
2. Apply +10 V between the + voltage input terminal ($+V_{in}$) and ground. Adjust R1 for f_{out} = 10 kHz on the 4731, 100 kHz on the 4733 and 1 MHz on the 4735.
3. Repeat (1) and (2) for precise Zero and Full Scale set. Note: Zero is set at 10 Hz, 100 Hz, and 1 kHz out for 10 mV in, because it is impractical to measure 0 Hz out for 0 V in.

Full Scale accuracy for the + current input is ±25%. Greater accuracy is obtained by using the Full Scale and Zero trim circuits shown in Figure 3.

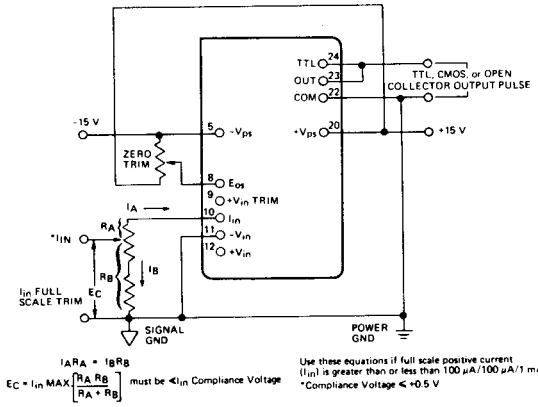


Figure 3. Zero & Full Scale Trim for Positive Input Currents

THEORY OF OPERATION

To take maximum advantage of the 4731/4733/4735's versatility (Figure 4) a functional block diagram and theory of operation is provided. With this information, input and output circuitry are easily modified to handle virtually any signal or load.

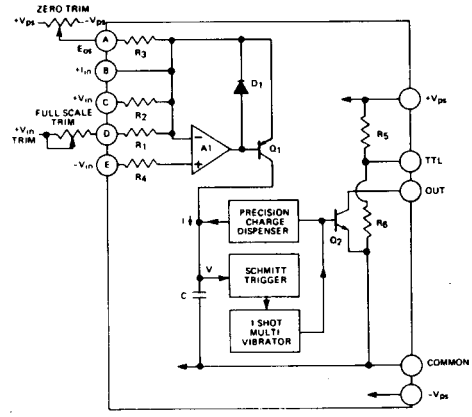


Figure 4. Models 4731/4733/4735 Simplified Block Diagram

The 4731/4733/4735 V-to-F is a free running (astable) voltage controlled multivibrator. See Figure 4. The effective currents from the four inputs (A, B, C, & D) are summed at the minus input of op amp A1. A1 and transistor Q1 form a precision current pump, producing current I from the collector of Q1, which is a linear function of the A1 input currents. Current I charges capacitor C at a rate which is a precise linear function of the V-to-F's input signal.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt-Trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a constant width output pulse. This pulse performs two functions. Amplified by Q2, it is the output of the V-to-F and functionally activiates the Precision Charge Dispenser (PCD). The PCD discharges C to the same "zero" level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the V-to-F input signal, producing the waveforms shown in the timing diagram, Figure 7. That is, the rate of charging C, (the repetition rate of charging C and thus the output frequency) are functions of the V-to-F voltage and/or current inputs.

TRIM THEORY

The V-to-F input circuit Zero and Full Scale trim techniques are based on the input circuit amp (A1, Figure 4) and the user may treat the input as such within certain limits. No combination of signals may be applied to the V-to-F inputs which will drive the A1 output positive. That is, a frequency output will not result if the total current into the V-to-F positive inputs (A1, summing point) becomes negative with respect to the V-to-F negative input. If this occurs, D1 will become forward biased, Q1 cut off, I becomes zero, and f_{out} becomes zero. The inherent current Full Scale Factor is 100 μA/100 μA/1 mA, ±25% to give 10 kHz/100 kHz/1 MHz out. All current trimming must take this ±25% tolerance into account. Resistor R1 is factory trimmed so that the $+V_{in}$ trim is within +1% full scale ±0.5%, i.e. +10 V at V_{in} trim input (4731) the output will be 10.1 kHz ±0.05 kHz. Resistor R2 is factory

trimmed so that $+V_{in}$ is within ±0.5%, i.e. +10 V at $+V_{in}$ input (4731) the output will be 10.0 kHz ±0.05 kHz. Both $+V_{in}$ inputs are trimmed with V_{cc} = ±15 V @ 25 °C.

FULL SCALE FACTOR CHANGE

The specified Full Scale Factor for the 4731/4733/4735 is 9.9 V±0.5% (or +100 μA/100 μA/1 mA, ±25%) to produce 10 kHz/100 kHz/1 MHz out. Many applications require 10 kHz/100 kHz/1 MHz for other (larger or smaller) Full Scale input signals and polarities. Figures 5A through 5F illustrate how to operate the 4731/4733/4735 with such signal levels.

Magnitude of $V_{IN} > 20$ V

These V-to-F's can be operated with input voltages greater than +20 V by connecting a fixed resistor and trim potentiometer in series with the + voltage input (see Figure 5A). For voltages more negative than −10 V, the attenuator network of Figure 5B performs well. Zero Trim and other adjustments remain the same as in Figure 2.

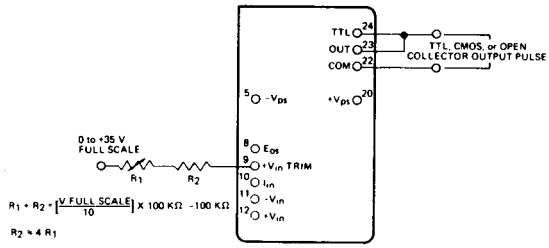


Figure 5A. Full Scale $+V_{in}$ Greater Than +20 V

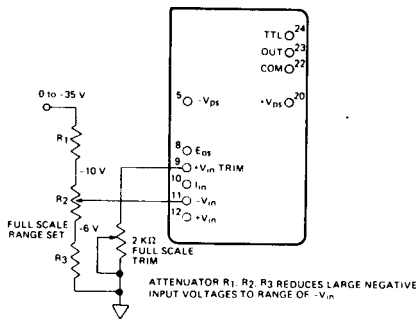


Figure 5B. Full Scale Input Voltage More Negative Than −8 V

−10 Volts < Full Scale V_{IN} < +10 Volts

If the full scale input voltage is between +10 μV and +1 V, (100 dB) the full scale output is set at 10 kHz/100 kHz/1 MHz by using the + current input terminal with a series resistor as shown in Figure 5C.

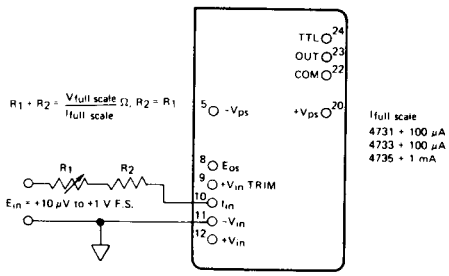


Figure 5C. Full Scale Input Between ≈ +10 μV and +1 V

When the Full Scale Input Signal is between −0.1 volts and +0.1 volts, a low drift amplifier such as the TP 1703 should be used to raise the signal to 10 V. See Figure 5D.

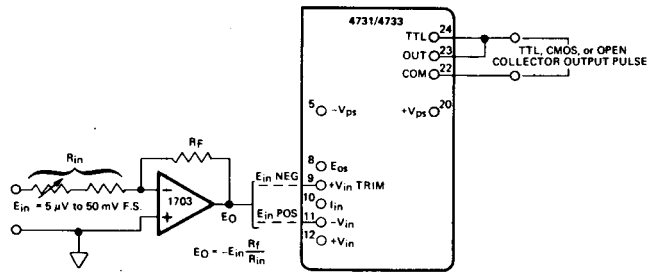


Figure 5D. Full Scale Input Voltage −.1 V and +.1 V

Reduce Full Scale f_{out} Below 10 kHz/100 kHz/1 MHz

In some applications, a Full Scale output frequency of less than 10 kHz/100 kHz/1 MHz is required when the input signal is 10 V or greater. The circuits of Fig. 5A-F and 6 which show attenuation of the input signal to 10 volts are used to decrease the Full Scale input signal below 10 V and, therefore, Full Scale f_{out} below 10 kHz/100 kHz/1 MHz.

To maximize use of the V-to-Fs dynamic range, however, the input signal is conditioned to + or −10 V Full Scale and a binary or BCD frequency divider (counter) is connected to the output. Any TTL or CMOS device may be used, from a simple divide by 10 unit such as the TTL 54/74 90A to a programmable divider such as the CMOS CD4059, which can divide by any number from 3 to 15,999.

If the 4731/4733/4735 FS output is set at 10 kHz/100 kHz/1 MHz, as shown in Figure 5E, counter output will be 1 kHz/10 kHz/100 kHz (minimum output frequency will be 1 mHz/10 mHz/100 mHz).

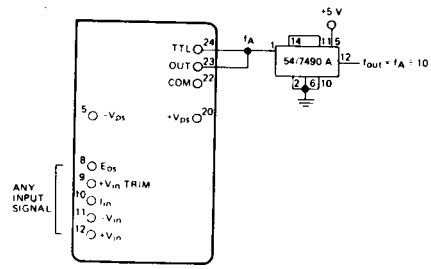


Figure 5E. Full Scale Output Less Than 10 kHz/100 kHz/1 MHz When V_{in} Is Equal To Or Greater Than 10 V

Full Scale Input Current Greater Than 100 μA/100 μA/1 mA

If the full scale input current is greater than 100 μA/100 μA/1 mA, the "current splitter" circuit of Figure 3 is used. As noted in Figure 3, the voltage developed at the wiper of the potentiometer must be less than the compliance voltage of the current source. A negative input current can be conditioned by passing it through a resistor connected between $-V_{in}$ and signal common, thus producing a negative voltage. (Trim per Figure 2B at $+V_{in}$.) The compliance voltage of the current source, however, must be greater than the maximum voltage developed across the resistor.

The best way to CONDITION CURRENT SIGNALS is with the classic current to voltage converter circuit shown in Figure 5F. With this circuit and the "right" amplifier virtually any current (even femtoamps) will provide a positive or negative 10 V full scale input to the V-to-F with no compliance voltage problem.

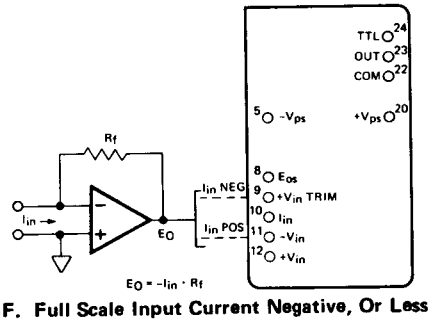


Figure 5F. Full Scale Input Current Negative, Or Less Than 200 μA/ 200 μA/2 mA

Differential Inputs

The V-to-Fs $+V_{in}$ and $-V_{in}$ terminals represent a true differential input capable of accepting a signal from a balanced line, a thermistor bridge or a signal source sitting at a common mode voltage. The V-to-F's differential input eliminates the need for a differential amplifier.

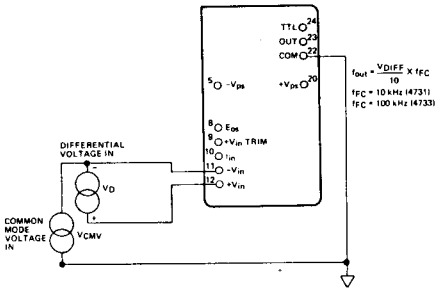


Figure 5G. Definition Of Differential & Common Mode Voltage

To use the V-to-F voltage inputs differentially, several simple conventions (definitions) must be observed as illustrated in Figure 5G.

1. Common Mode Voltage (CMV) is defined as the voltage between $\pm V_{CC}$ common and the negative V_{in} pin.
2. The positive V_{in} pin must always be positive with respect to the negative V_{in} pin.
3. CMV Range is typically between $+V_{CC}$ −4 and $-V_{CC}$ +5 V.
4. The differential (floating, balanced) signal source must be returned to $+V_{CC}$ common and must not create voltages which exceed the limits set by 1, 2, and 3.
5. $$f_{out} = \frac{(+V_{in}) - (-V_{in}) \times f_A}{10\ V}$$ f_A = 10 kHz (4731), f_A = 100 kHz (4733), f_A = 1 MHz (4735)

CMOS Logic

The 4731/4733/4735 output circuit is easily adapted to drive CMOS. It is only necessary to parallel R5 (Figure 4) with a 1 kΩ resistor. This additional pull-up resistor also decreases pulse rise time to drive larger capacitive loads. If pin 23 is not connected to pin 24, an external divider must be provided.

BIPOLAR SIGNALS–SCALE EXPANSION–FAST SIGNALS

Operate with Bipolar Input Signals

The V-to-F can not operate with bipolar (e.g., −5 V to +5 V) input signals when connected as shown in Figures 1 and 2. To handle such inputs, it is necessary to offset the zero. That is, produce a pulse train out for "zero" volts in. For example: If the $+V_{in}$ pin is connected to zero volts and the $-V_{in}$ pin is connected to a fixed −5 volts, the output of the V-to-F has been "offset" to 5 kHz/50 kHz/ .5 MHz. If the $+V_{in}$ pin is now connected to −5 V, f_{out} is 0 kHz; if $+V_{in}$ is zero, f_{out} is 5 kHz/50 kHz/.5 MHz; if $+V_{in}$ is +5V, f_{out} is 10 kHz/100 kHz/1 MHz. The offsetting may be performed at the $+V_{in}$ pin and the signal applied to the $-V_{in}$ pin or the $+I_{in}$ pin; or the $+I_{in}$ pin may be used for the fixed offset. Offsetting may be combined with all of the techniques of Figures 5 and 6 to provide versatile signal conditioning.

Expand a Portion of Scale to Full Scale

An input signal is often a small voltage change impressed on a larger fixed voltage. This situation is handled by nulling (offsetting) the DC or unchanging component of the input signal at one input and adjusting the Full Scale Gain Factor at another so the variable portion of the input signal causes the output frequency to cover the full excursion from 0 Hz to 10 kHz/100 kHz/1 MHz. Such a signal is a voltage level which varies between +4 and +6 volts. To implement offsetting, connect $+V_{in}$ to −4 V. Since the actual signal is 2 V (6 V −4), connect it to $+I_{in}$ in series with resistor and trim pot to generate 100 μA/100 μA/ 1 mA with 2 V.

When the input varies between +5 V and +15 V (signal = 10 V), implement offsetting by connecting $-V_{in}$ to +5 V and apply signal to $+V_{in}$. Trim per Figure 4. If the input varies between +30 V and +50 V (signal = 20 V), implement offsetting by connecting −30 V to $+I_{in}$ through a 150 kΩ resistor and series pot. Connect the signal to $+V_{in}$ through a 100 kΩ resistor and series pot. Ground the $-V_{in}$ input.

Operate With Fast Signals

A V-to-F application may require operation with rapidly changing input signals. For example, the output of a load cell may change from 0 to Full Scale (or Full Scale to 0) in 1 ms. To accurately handle this signal, the output of the V-to-F must be able to change faster than the input.

The basic response or settling time of the 4731/4733/4735 for any step input is one period of the new frequency plus 5 μs. That is, if the input is changed from 10 volts to 0.001 volts, the new frequency is one/ten/hundred Hertz and response time is one second/.1 second/.01 second +5 μsec. When the input changes from 11 volts to 10 volts, the new frequency is 10 kHz/100 kHz/1 MHz, one period is 100 μsec/10 μsec/1 μsec, and response time is 105 μsec/15 μsec/6 μsec. Therefore, if the V-to-F input signal changes between 0 and Full Scale in one millisecond, the output frequency of the V-to-F for zero volts in must be offset to a new frequency, the period of which is less than the one millisecond required for the input to change.

The Full Scale value of the input signal is then adjusted so the V-to-F will operate between this offset or zero frequency and the maximum Full Scale frequency. In Figure 6 a zero to +1 volt signal is shown providing an output frequency which will vary between 9 kHz and 10 kHz/ 90 kHz and 100 kHz/900 kHz and 1 MHz.

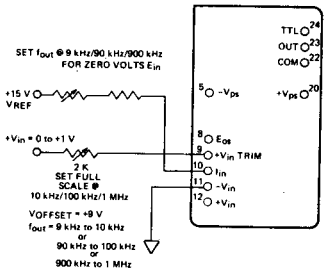
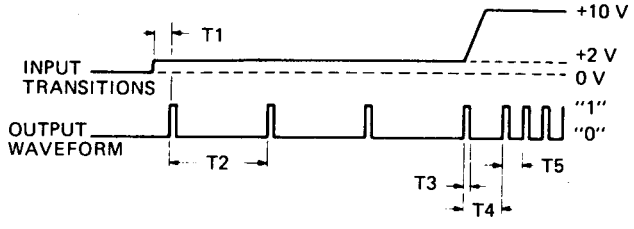


Figure 6. Frequency Offset @ 9 kHz/90 kHz/900 kHz To Decrease Settling Time

HOW TO USE 4731/4733/4735 OUTPUT

The TTL LOGIC pulse train from the V-to-F is designed to drive at least one TTL load over the power supply range +9 V to +18 V. At +15 volts, it can drive 10 TTL loads. The output circuit (see Figure 4) is a single transistor Q2 connected as a saturated switch with pull up resistor R5. When Q1 is on, the output is at "zero" volts. When Q2 is off, the output voltage is $+V_{CC}/3$ (assuming pins 23 and 24 are connected) or +5 V when $+V_{CC} = +15$.



Typical Time in Micro-Seconds

	T1	T2	T3	T4	T5
4731	0 to 500	500	20	≈200	100
4733	0 to 50	50	2	≈30	10
4735	0 to 5	5	0.2	≈3	1

Figure 7. Typical Waveforms, Showing Timing Relationships

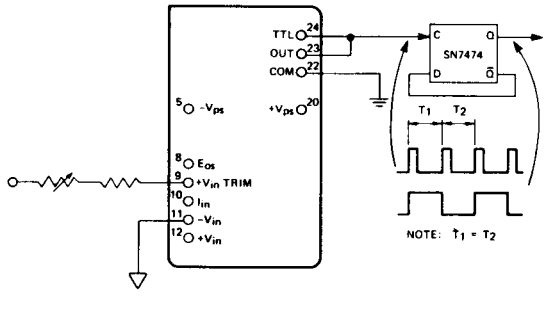


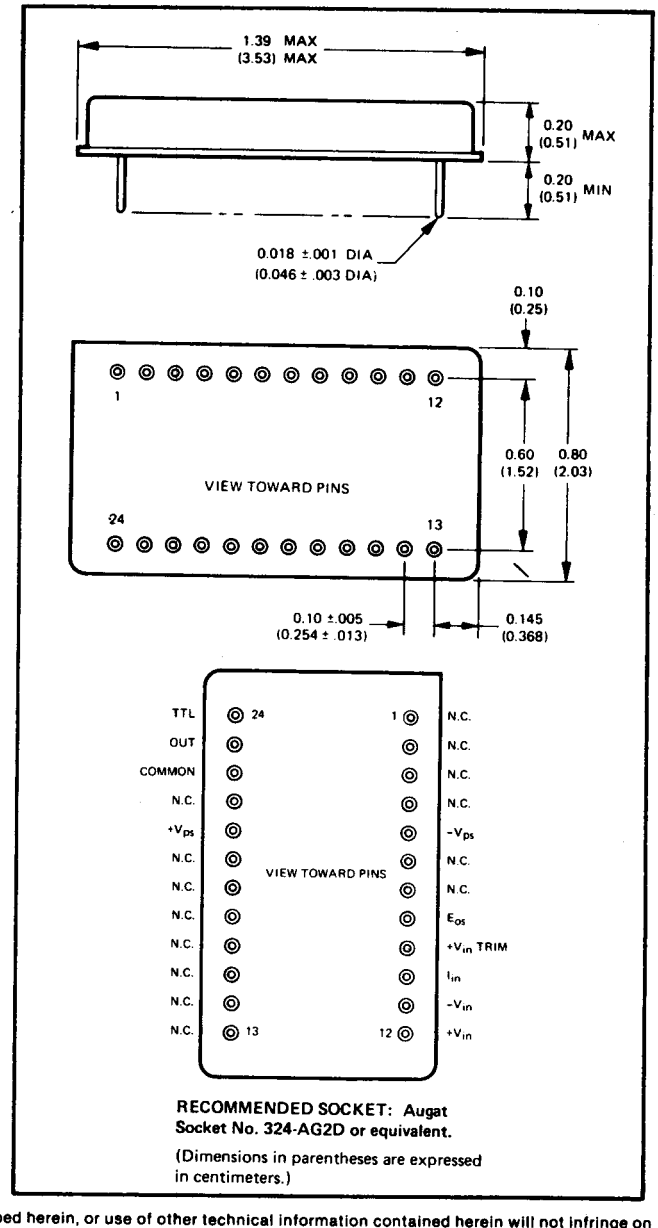
Figure 8. Square Wave Output Using D - Type Flip Flop

Output Protection ($+V_{CC}$, Common, $-V_{CC}$)

The V-to-F output (collector of Q2) may be shorted to ground indefinitely without damage, however, since Q2 is ON most of the time, a short to $+V_{CC}$ will cause certain catastrophic failure in about 5 seconds. A short to TTL (pin 24) and $-V_{CC}$ simultaneously will cause instant catastrophic failure.

Square Wave Output

The output of the 4731/4733/4735 is a train of pulses 20 μsec/2 μsec/.2 μsec (see Figure 7). A symmetrical (square wave) output for driving highly capacitive or noisy transmission lines is obtained with a D or JK flip flop as shown in Figure 8.



RECOMMENDED SOCKET: Augat Socket No. 324-AG2D or equivalent.

(Dimensions in parentheses are expressed in centimeters.)

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