

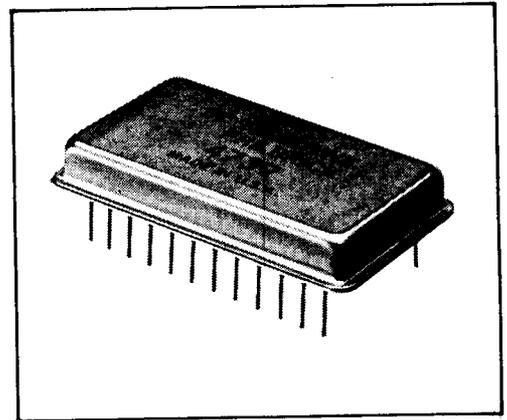
# 5MHz and 10MHz Hybrid Voltage to Frequency Converters

# 4739 4743

The 4739 and 4743 are Philbrick's newest hybrid voltage to frequency converters. Offering full scale outputs of 5MHz and 10MHz, respectively, the 4739 and 4743 can be externally trimmed to any value from their rated full scale outputs down to 2.5MHz. Both units have full differential input capabilities and can be driven with positive voltages, negative voltages, or positive currents. Common mode rejection ratio, with CMV = 10 volts, is 80dB. With external resistors, the input is easily adapted to accept almost any input signal range. The output stages of both units are single uncommitted transistors that operate as saturated switches. Pull-up resistors for TTL compatibility are internal to the 4739's and 4743's 24 pin welded-metal dual-in-line packages. External resistors can be added to make the outputs CMOS compatible. Both units are capable of driving 10 TTL loads.

Dynamic range for both units is greater than 100dB, and input/output linearity is specified over a  $\pm 10\text{mV}$  to  $\pm 10.5\text{V}$  input range. For the 4739, the spec is  $\pm 0.05\% \text{FS}$  plus  $\pm 0.001\%$  of signal. For the 4743, the spec is  $\pm 0.05\% \text{FS}$  plus  $\pm 0.05\%$  of signal. Initial zero offset error is  $\pm 8\text{mV}$  (4kHz) for the 4739 and  $\pm 8\text{mV}$  (8kHz) for the 4743. Zero Offset error is externally adjustable to zero. Initial full scale accuracy for both units is  $\pm 50\text{kHz}$ , and full scale error is also externally adjustable to zero. If full scale adjusting is not employed, pins 7 and 9 must be tied together.

The 4739 and 4743 both have quick response times, settling to within  $\pm 0.01\% \text{FS}$  of a new frequency in  $15\mu\text{sec}$ . Overload recovery time for both units is approximately 10 output signal periods. Both units operate from  $\pm 14\text{V}$  to  $\pm 18\text{V}$  supplies and are specified for  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  operation. Please contact the factory for specified  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  operation and MIL-STD-883 screening.



## FEATURES

- 5MHz (4739) and 10MHz (4743) Full Scale Outputs
- Full Differential Input
- 100dB Dynamic Range
- Nonlinearity: 4739/4743  $\pm 0.05\% \text{FS}$  plus  $\pm 0.001\%$  Signal  $\pm 0.05\% \text{FS}$  plus  $\pm 0.05\%$  Signal
- $\pm 14\text{V}$  to  $\pm 18\text{V}$  Supplies
- 24 Pin Hermetic DIP
- Easily Modified for Different Input/Output Signals

## APPLICATIONS

- Two-Wire Digital Data Transmission
- Ratiometric Data Conversion
- Long Term Integrators
- Fiber Optic Data Links
- FM Modulation

**ABSOLUTE MAXIMUM RATINGS**

± 15V Supply Voltage ( ± V <sub>CC</sub> , Pins 20, 5)	± 22 Volts
Analog Input Voltage (Pins 11, 12) (Note 1)	± 15 Volts
Differential Input Voltage (Pins 11, 12)	± 30 Volts
Operating Temperature Range	- 55°C to + 125°C
Specified Temperature Range:	
4739/4743	0°C to + 70°C
4739-83/4743-83 (Note 2)	- 55°C to + 125°C
Storage Temperature Range	- 65°C to + 150°C

**SPECIFICATIONS** (T<sub>A</sub> = + 25°C, ± V<sub>CC</sub> = ± 15V, unless otherwise indicated)

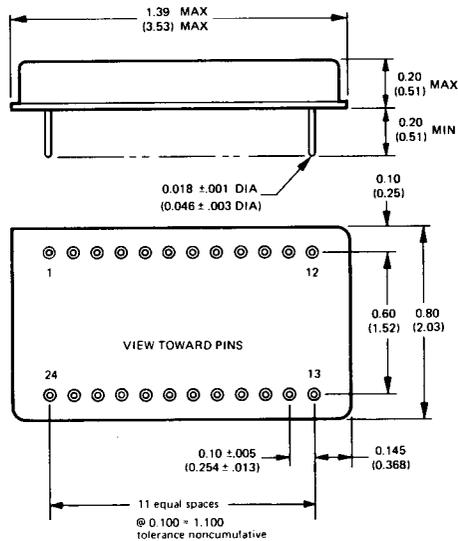
PARAMETER	4739	4743	UNITS
<b>ANALOG INPUTS</b>			
Input Range: + V <sub>in</sub>	+ 100μV to + 10.5V	+ 100μV to + 10.5V	
- V <sub>in</sub>	- 100μV to - 10.5V	- 100μV to - 10.5V	
+ V <sub>in</sub> - (- V <sub>in</sub> )	± 100μV to ± 10.5V	± 100μV to ± 10.5V	
+ I <sub>in</sub>	+ 0.1μA to 1mA	+ 0.1μA to 1mA	
Overrange	20	10	%
Input Impedance: + V <sub>in</sub>	10	10	kΩ
- V <sub>in</sub>	20	20	kΩ
+ I <sub>in</sub>	Virtual Ground	Virtual Ground	
Common Mode Voltage	± (V <sub>CC</sub> - 5)	± (V <sub>CC</sub> - 5)	Volts
Common Mode Rejection Ratio	80	80	dB
Dynamic Range	100	100	dB
<b>FREQUENCY OUTPUT</b>			
Full Scale Frequency	5	10	MHz
Output Waveform (Note 3): High Level	5	5	Volts
Low Level	0.4	0.4	Volts
Fanout	10	10	TTL Loads
Pulse Width	50 to 75	45 to 65	nsec
Output Impedance	666 ± 5%	666 ± 5%	Ω
<b>TRANSFER CHARACTERISTICS</b>			
Nonlinearity: + V <sub>in</sub> (+ 10mV to + 10.5V)	± 0.05 ± 0.001	± 0.05 ± 0.05	%FS plus %Signal
- V <sub>in</sub> (- 10mV to - 10.5V)	± 0.05 ± 0.001	± 0.05 ± 0.05	%FS plus %Signal
+ I <sub>in</sub> (1μA to 1mA)	± 0.05 ± 0.001	± 0.05 ± 0.05	%FS plus %Signal
Offset Error	± 0.08	± 0.08	%FS
Full Scale Error	± 50(± 1.0)	± 50(± 0.5)	kHz(%FS)
<b>STABILITY</b>			
Offset Drift	± 100	± 100	μV/°C
Offset Power Supply Sensitivity	± 20	± 20	μV/%ΔV <sub>CC</sub>
Full Scale Drift	± 75	± 100	ppm/°C
Full Scale Power Supply Sensitivity	± 75	± 125	ppm/%ΔV <sub>CC</sub>
<b>DYNAMIC CHARACTERISTICS</b>			
Response Time (10V Input Step to ± 0.01%)	15	15	μsec
Overload Recovery Time (+ V <sub>in</sub> = + 20V to + 10V)	10	10	Cycles
<b>POWER SUPPLIES</b>			
Power Supply Range	± 14 to ± 18	± 14 to ± 18	Volts
Current Drain	+ 75, - 25	+ 75, - 25	mA
Power Supply Asymmetry	± 4	± 4	Volts
Power Consumption	1500	1500	mW

**Notes:** 1. For supply voltages less than ± 15V, the input voltage cannot exceed the supply voltage.

2. The 4739-83 and 4743-83 are specified for - 55°C to + 125°C operation and screened to the requirements of MIL-STD-883, Method 5008. Please contact factory.

3. The 4739 and 4743 can withstand an indefinite short to ground or to + V<sub>CC</sub> for 5 seconds without damage or degradation to performance. However, both units will fail if shorted to the - V<sub>CC</sub> supply.

**Package Dimensions**

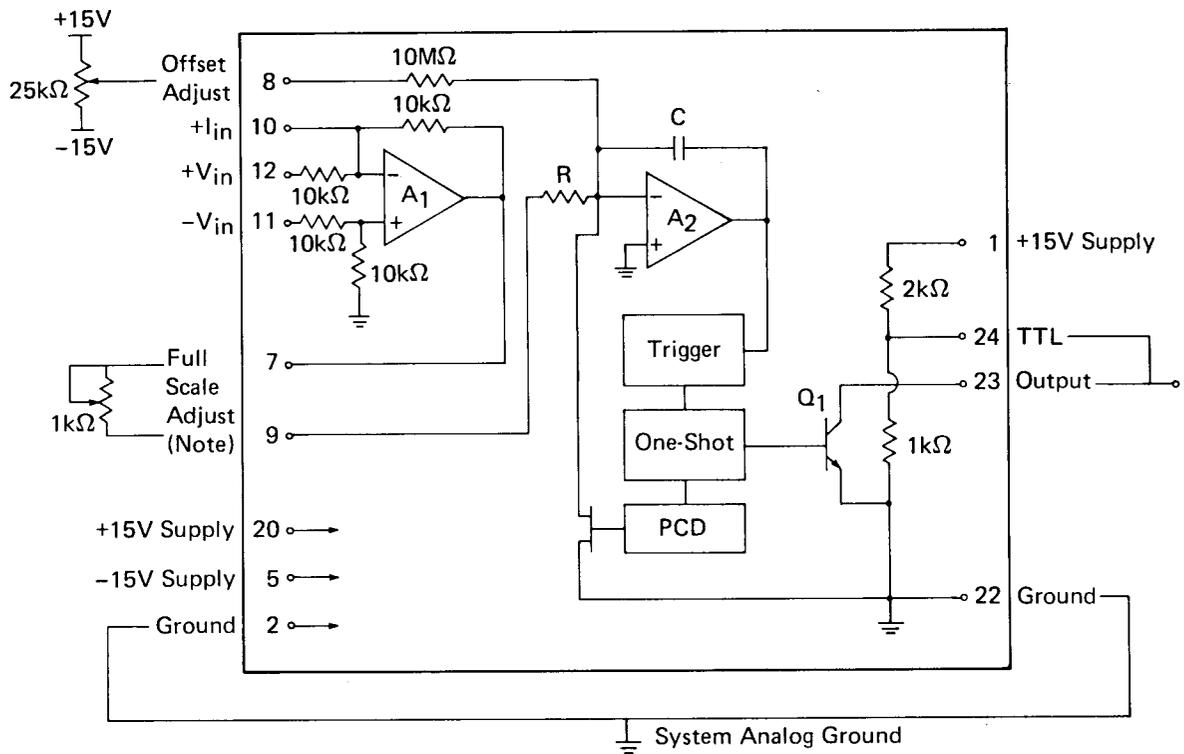


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**Pin Designations**

Pin 1	+ 15V Supply (+ V <sub>CC</sub> )	Pin 24	TTL
Pin 2	Ground	Pin 23	Output
Pin 3	N/C	Pin 22	Ground
Pin 4	N/C	Pin 21	N/C
Pin 5	- 15V Supply (- V <sub>CC</sub> )	Pin 20	+ 15V Supply
Pin 6	N/C	Pin 19	N/C
Pin 7	Full Scale Adjust	Pin 18	N/C
Pin 8	Offset Adjust	Pin 17	N/C
Pin 9	Full Scale Adjust	Pin 16	N/C
Pin 10	+ I <sub>in</sub>	Pin 15	N/C
Pin 11	- V <sub>in</sub>	Pin 14	N/C
Pin 12	+ V <sub>in</sub>	Pin 13	N/C

**4739/4743 Block Diagram**



NOTE: If external full scale accuracy adjustment is not used, pins 7 and 9 must be tied together.

### Description of Operation

To take maximum advantage of the 4739/4743's versatility, a functional block diagram and theory of operation are provided. With this information, input and output circuitry are easily understood and easily adapted to handle virtually any signal or load.

The 4739/4743 are free-running (astable) voltage controlled multivibrators. A true differential input amplifier ( $A_1$ ) allows the devices to be driven by positive input voltages applied to pin 12 (with pin 11 open or grounded), by negative voltages applied to pin 11 (with pin 12 open or grounded), by differential voltages applied between pins 12 and 11 ( $V_{in} = +V_{in} - (-V_{in})$ ), or by positive current applied to pin 10. CMRR at  $CMV = 10V$  is typically 80dB. No combination of input signals that will drive the  $A_1$  output positive is permitted.

Operating under any of the allowed input conditions, the result is a negative voltage at the output of  $A_1$ . Resistor  $R$ , amplifier  $A_2$ , and capacitor  $C$  form an integrator.  $C$  charges as a precise linear function of the V/F's input signal. When the voltage (charge) impressed on  $C$  reaches a fixed precise threshold, the trigger circuit triggers the one-shot (monostable) multivibrator, which in turn produces a constant-width output pulse. This pulse performs two functions. Amplified by  $Q_1$ , it becomes the output of the V/F. At the same time, it activates the precision charge dispenser (PCD). The PCD discharges  $C$  to the same "zero" level every time an output pulse is produced. Thus, capacitor  $C$  is repeatedly charged between two precise voltages at a rate which is a linear function of the V/F input signal. That is, the rate of charging  $C$ , the repetition rate of charging  $C$ , and the output frequency are all functions of the V/F voltage and/or current inputs.

### Offset and Full Scale Trim Theory

Zero offset and full scale trim techniques are based on the input circuit. Offset is adjusted with a 25k $\Omega$  potentiometer between  $+V_{CC}$  and  $-V_{CC}$ , with its wiper tied to pin 8. The subsequent voltage applied to pin 8 falls across a 10M $\Omega$  resistor to become a constant positive or negative current directly injected into the integrator capacitor. Full scale is adjusted by varying the integrator's input resistor with a 1k $\Omega$  rheostat connected between pins 7 and 9. This adjustment procedure can only lower the V/F's full scale output frequency, so units are laser trimmed at the factory to have initial full scale output errors that are always positive. By placing a fixed resistor in series with the adjusting rheostat, the 4739's and 4743's full scale output frequencies can be lowered to 2.5MHz. If full scale adjustment is not employed, pins 7 and 9 must be tied together with as short a jumper as possible.

### 4739/4743 Output Circuit

The TTL logic pulse train from the V/F is designed to drive 10 TTL loads with  $\pm 15V$  supplies. The output circuit is a single transistor ( $Q_1$ ) connected as a saturated switch with an uncommitted 2k $\Omega$  pull-up resistor. With pins 23 and 24 connected together, the output is approximately zero volts when  $Q_1$  is on. With  $Q_1$  off, the output voltage is  $+V_{CC}/3$  or +5V when  $+V_{CC} = +15V$ . If pin 23 is not connected to pin 24, an external divider must be provided. The output circuit is easily adapted to drive CMOS logic by paralleling the 2k $\Omega$  resistor with an external resistor large enough to bring the output up to the desired level. The additional pull-up resistor also decreases pulse rise time when driving larger capacitive loads.

The 4739/4743's output (collector of  $Q_1$ ) may be shorted to ground indefinitely without damage—however, since  $Q_1$  is on most of the time, a short to  $+V_{CC}$  will cause certain catastrophic failure in about 5 seconds.

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**TELEDYNE PHILBRICK**

Allied Drive @ Rte. 128, Dedham, Massachusetts 02026  
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439