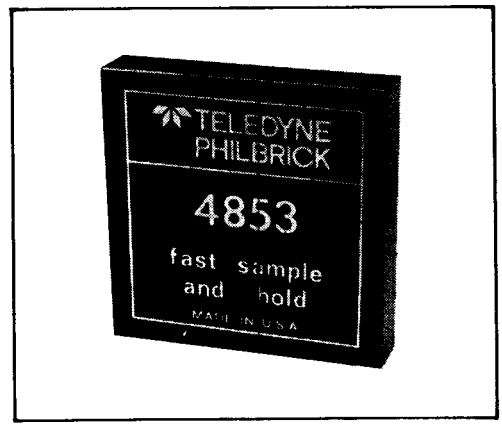
TELEDYNE PHILBRICK

High Speed Low Phase Shift Sample-Hold Amplifier

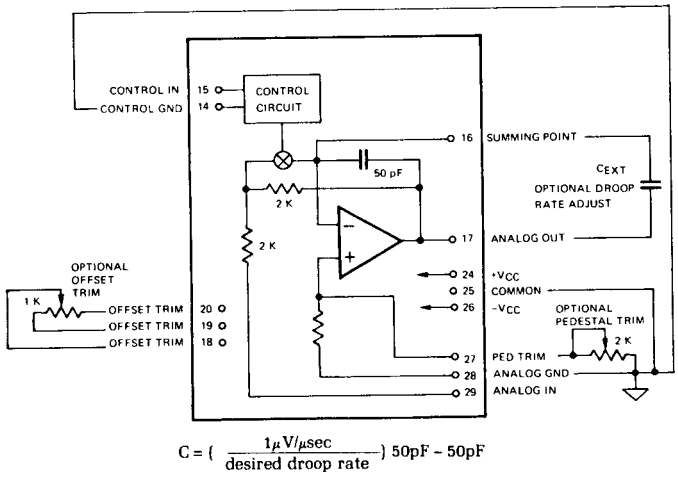
4853

The 4853 is a precision, high speed sample-hold amplifier. Its 1μsec acquisition time (to ±0.01%), ±1nsec aperture jitter, and 300nsec sample-hold settling time (to ±0.01%) permit its use with fast 12 bit A/D and D/A converters. Its low phase shift and feed-through characteristics make it ideally suited for high frequency, multiplexed data acquisition systems.



Accuracy Trimming

The output offset voltage in either the sample or hold mode may be trimmed to zero while cycling between sample and hold with the input grounded by adjusting the 1kΩ offset trim potentiometer (shown in Figure 1) for 0V output. This procedure does not reduce pedestal. A negative pedestal may be trimmed to zero while cycling between sample and hold with the input grounded by adjusting the 2kΩ pedestal trim potentiometer. A positive pedestal may be trimmed to zero by adding a small external capacitor, typically 2pF, between pin 16 and pin 17. If adding this capacitor makes the pedestal slightly negative, use the trim procedure described above. Note: the external capacitance will increase acquisition time. See Figure 3. The output droop rate can be adjusted to a desired value by adding external capacitance between pins 16 and 17 (formula given in Figure 1). For optimal performance, the external capacitor should be either a teflon or polystyrene type. Adding this capacitor will increase acquisition time and make the pedestal more negative. See Figures 3 and 4.



$$C = \left(\frac{1\mu V/\mu sec}{\text{desired droop rate}} \right) 50pF - 50pF$$

Figure 1. Functional Block Diagram

FEATURES

- 0.01° Phase Shift @ 20kHz
- 1μsec Acquisition Time
- 300nsec Settling Time
- ±0.005% Non-Linearity
- Adjustable Pedestal and Droop
- Internal Electrostatic Shielding

APPLICATIONS

- Data Acquisition Systems
- Analog Memories
- Data Distribution Systems
- Deglitch Circuits

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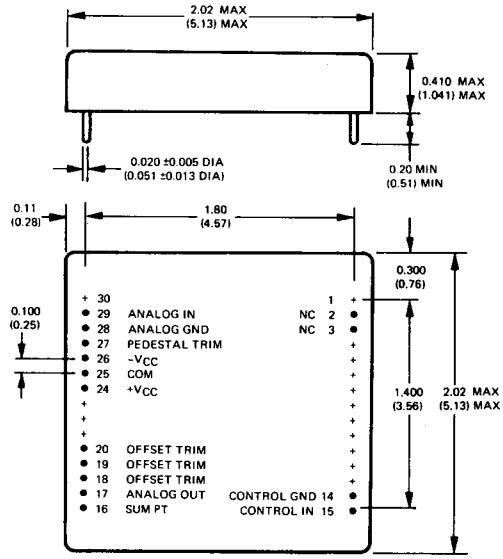
SPECIFICATIONS (At 25°C, ±15V, unless otherwise indicated)

	Typical	Guaranteed
INPUTS		
Analog		
Voltage	±11V	±10V
Bias Current	±5mA	---
Impedance	2kΩ || (20pF series 2kΩ)	
Power		
Voltage nominal, $\pm V_{CC}$	---	±15V ±2%
Voltage range, $\pm V_{CC}$	---	±10V to ±18V
Current (Quiescent)	---	±30mA
Digital		
Hold Mode	---	≤ +0.8V
Sample Mode	---	≥ +2.0V
Loading ①	---	1 TTL Load
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity ⑥	±0.003% of F.S.	±0.005% of F.S.
Gain (nominal at DC)	−1.000	---
Gain Error ② ⑦	±0.02%	±0.05%
Sample Voltage Offset ③	±1mV	±3mV
Pedestal Voltage ③	±1mV	±3mV
Hold Jump Voltage ③	---	±1mV
Decay Rate in Hold ④	---	±1μV/μsec
Feedthrough in Hold ⑧	---	1mVp-p
Stability		
Gain vs Temp ②	±5ppm/°C	±10ppm/°C
Sample Voltage Offset vs Temp	±75μV/°C	±150μV/°C
Hold Voltage Offset vs Temp	±100μV/°C	±200μV/°C
PSRR (Tracking)	---	±0.001%/%ΔV
(Non-Tracking)	±0.01%/%ΔV	---
Long Term Stability	±0.01%/year	---
Warm-up Time	10 minutes	---
Dynamic Characteristics		
Bandwidth (referred to DC gain)		
0.02%	to 20kHz	---
0.1%	to 80kHz	---
Slew Rate	30V/μsec	---
Aperture Delay Time ⑤	---	10nsec
Aperture Time ⑤	---	4nsec
Aperture Jitter	---	±1nsec
Acquisition Time		
10V step to 0.01% of F.S.	800nsec	1μsec
10V step to 0.1% of F.S.	600nsec	---
20V step to 0.01% of F.S.	1.2μsec	1.5μsec
20V step to 0.1% of F.S.	1μsec	---
Sample to Hold Transient	20mV	---
Settling Time, Sample to Hold		
to 0.01% of F.S.	200nsec	300nsec
to 0.1% of F.S.	100nsec	---
Phase Shift at 20kHz	---	0.01°
OUTPUT		
Voltage	±11V	±10V
Current	±20mA	±15mA
Resistance	0.02Ω	---
ENVIRONMENTAL SPECIFICATIONS		
Operating Temperature Range	---	0 to +70°C
Storage Temperature Range	---	-55 to +125°C
Relative Humidity	95% non-condensing	---
ABSOLUTE MAXIMUM RATINGS		
Supply Voltages to Ground	---	±18V
Digital Input Voltage	---	+5.5V
Analog Input Voltage	---	$\pm V_{CC}$
Short Circuit Protection		
Analog Output to Ground	---	Indefinitely

① A standard TTL unit load is −1.6mA max. at ≤ +0.8V and +40μA max. at ≥ +2.0V.
② Input test signal DC to 20kHz, 20VP-P sine wave.
③ Trimmable to zero. Best case trim conditions for Voltage Offsets and Hold Jump Voltage may not occur simultaneously.
④ May double for each +10°C rise in ambient temperature.
⑤ Input test signal 25kHz, 10VP-P sine wave.
⑥ Full Scale is considered to be 10V, therefore 0.01% is 1mV.
⑦ To trim positive gain error, use a 10Ω potentiometer in series with the Analog Input.
⑧ Input test signal 20kHz, 10VP-P sine wave.



±0.01 Non-cumulative tolerance between pins
±0.02 Tolerance from case edge to center of pins

DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS

Figure 5. Mechanical Specifications

Guard Ring

To minimize current leakage all component leads connected to the summing point should be as short as possible and the summing point circuitry guarded on the circuit board with a grounded foil pattern. If the summing point pin is not used, it should be clipped off at the module base.

When used in an environment subject to strong electrostatic fields, a ground shield should be added to the circuit board on which the module is mounted. See Figure 2.

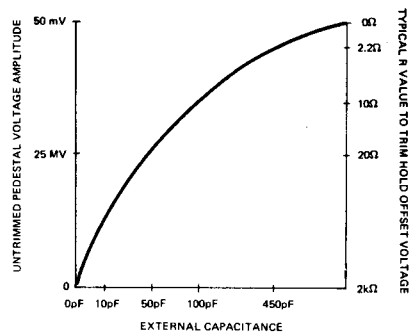


Figure 4. Pedestal Voltage and Trim R vs. External Capacitance

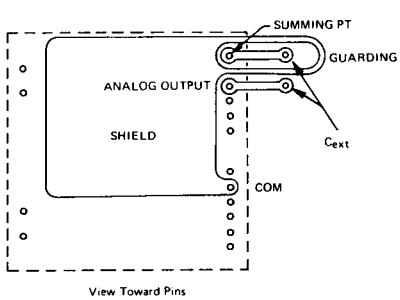


Figure 2. Shielding & Grounding

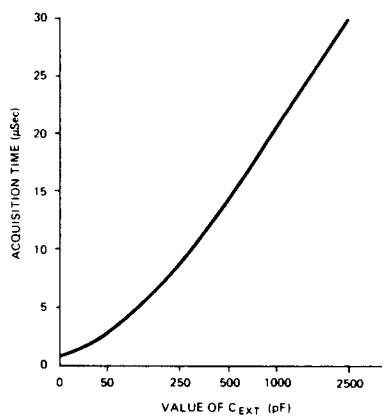


Figure 3. Effect of External Capacitance on Acquisition Time

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