Low Droop
Low Feedthrough
Sample-Hold Amplifier

4854

For moderate speed sample-hold applications, the 4854's combination of low cost, low droop, low feedthrough, high input resistance, and 10μsec acquisition time is unmatched. Applications requiring 0.1% (8 bit) overall accuracy need no trimming, and 0.01% (12 bit) accuracy is achieved with only an offset trim, thereby providing economy in installation time and effort. The 4854 uses the double inversion technique with the hold capacitor in the feedback path of the output amplifier (see Block Diagram). This method permits the switch to operate at ground potential, thereby minimizing switching time, aperture uncertainty, pedestal error, and leakage problems.

Applications Information

Power supplies should be externally bypassed to ground with 1μF tantalum capacitors in parallel with 0.01μF disc capacitors. Analog and digital grounds are internally connected to each other and should both be externally connected to system analog ground. The offset voltage in either the "hold" or "sample" mode may be trimmed to 0 volts while cycling between sample and hold with 0 volts input and adjusting the 1kΩ potentiometer, shown in Figure 1, for 0 volts output. At least 10 minutes warm-up time before trimming is recommended. Droop rate can be reduced by adding an external capacitor. The formula for determining its value is:

$$C_{ext} = \left(\frac{50\mu V/msec}{\text{Required Decay Rate}} \cdot 0.001\mu F \right) - 0.001\mu F$$

The external capacitor will cause an increase in acquisition time (see graph). Use low dielectirc absorption polystyrene or teflon capacitors and locate them close to the unit to reduce stray inductance. It should also be noted that AC feedthrough becomes lower as this external capacitance is increased. To minimize leakage currents, we recommend that leads of all components connected to the summing point be as short as possible and that the summing point circuitry be guarded with a grounded foil pattern. If the summing point pin is not used, it should be clipped off at the module base. Where the 4854 is used in an environment subject to strong electrostatic fields, a ground shield should be added to the circuit board on which the module is mounted.
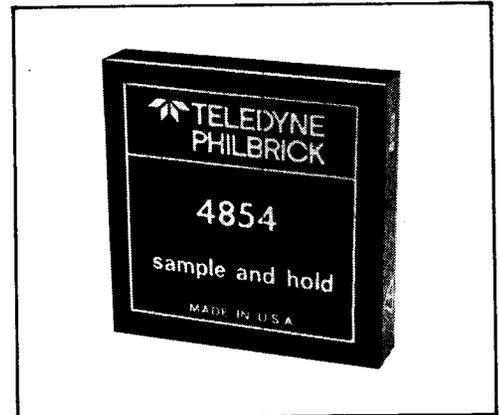
FEATURES

- Low Cost
- Internal Hold Capacitor
- Excellent 10μV/msec Droop
- 86db Feedthrough Attenuation
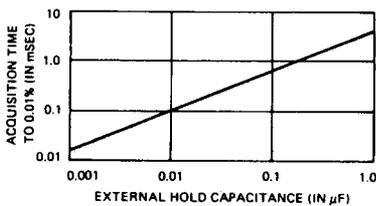- 10μsec Acquisition Time
- 1000MΩ Input Resistance

APPLICATIONS

- Data Acquisition Systems
- Peak Detectors
- Analog Memories
- Simultaneous Sample-Hold
- Data Distribution Systems

SPECIFICATIONS (At +25°C, ±15 Vdc, unless otherwise indicated)

|	TYPICAL	GUARANTEED
INPUTS		
Analog		
Voltage	±12 V	±10 V
Bias Current	±70 nA	±250 nA
Resistance	$10^9 \Omega$	---
Power		
Voltage, ±V_{CC}	---	±15 V ±1%
Current (Quiescent)	±13 mA	±20 mA
Recommended Philbrick Supply	2211	
Digital		
Hold Level	---	≤0.8 V
Sample Level	---	≥2.0 V
Loading ①	---	1 TTL Load
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity	±0.005% of F.S.	---
Gain	+1.000	---
Gain Error	---	±0.01% of F.S.
Sample Voltage Offset ④	±2 mV	±10 mV
Hold Voltage Offset ② ④	±5 mV	±15 mV
Hold Jump Voltage ②	±3 mV	±5 mV
Decay Rate in Hold ③	10 µV/msec	50 µV/msec
Feedthrough in Hold ⑤	400 µV P-P	1 mV P-P
Stability		
Gain vs. Temp.	±0.3 ppm/°C	---
Sample Voltage Offset vs. Temp.	±10 µV/°C	±30 µV/°C
Hold Voltage Offset vs. Temp.	±50 µV/°C	---
PSRR	±10 µV/%∆V_{CC}	---
Dynamic Characteristics		
Bandwidth, (−3 dB)	30 kHz	---
Bandwidth, 0.01% of F.S.	2.5 kHz	---
Bandwidth, 0.05% of F.S.	5 kHz	---
Bandwidth, 0.2% of F.S.	10 kHz	---
Slew Rate	1.5 V/µsec	---
Aperture Delay Time	---	40 nsec
Aperture Time	---	10 nsec
Aperture Uncertainty Time	±2 nsec	±4 nsec
Acquisition Time ③		
10 V Step to 0.01% of F.S.	12 µsec	---
10 V Step to 0.1% of F.S.	10 µsec	---
20 V Step to 0.01% of F.S.	18 µsec	---
20 V Step to 0.1% of F.S.	15 µsec	---
Sample to Hold Transient	150 mV	---
Settling Time, Sample to Hold		
To 0.01% of F.S.	1.5 µsec	---
To 0.1% of F.S.	1.2 µsec	---
Phase Shift, at 1 kHz	0.01°	---
Phase Shift, at 10 kHz	0.1°	---
OUTPUT		
Voltage, R_L = 2 KΩ	±12 V	±10 V
Current, E_{out} = ±10 V	±7 mA	±5 mA
Resistance (DC to 100 Hz)	0.01Ω	---
ENVIRONMENTAL SPECIFICATIONS		
Operating Temperature Range	---	0 to +70°C
Storage Temperature Range	---	−55 to +125°C
Relative Humidity	95% non-condensing	---
ABSOLUTE MAXIMUM RATINGS		
Supply Voltages to Ground	---	±18 V
Digital Input Voltage	---	+5.5 V
Analog Input Voltage	---	±V_{CC}
Short Circuit Protection		
Output to Ground	---	Indefinite

① A standard TTL unit load is −1.6 mA max. at ≤ +0.8 V and +40 µA max. at ≥ +2.0 V.
② External Capacitance will decrease Voltage Offset and Hold Jump Voltage.
③ Adding external capacitance will lower Decay Rate and increase Acquisition Time.
④ Trimmable to zero.
⑤ At 10 kHz sine, 20 V P-P
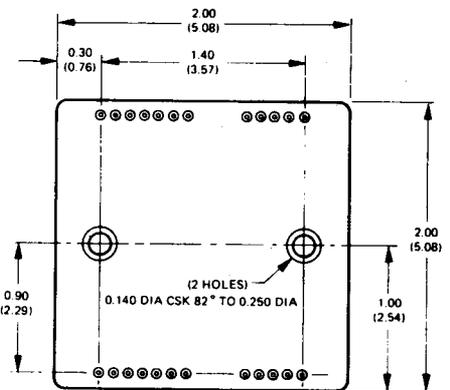

Effect of External Capacitance on Acquisition Time
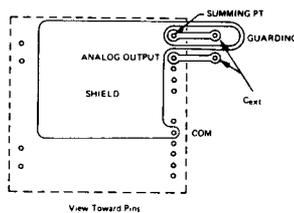
Shielding and Guarding
View Toward Pins
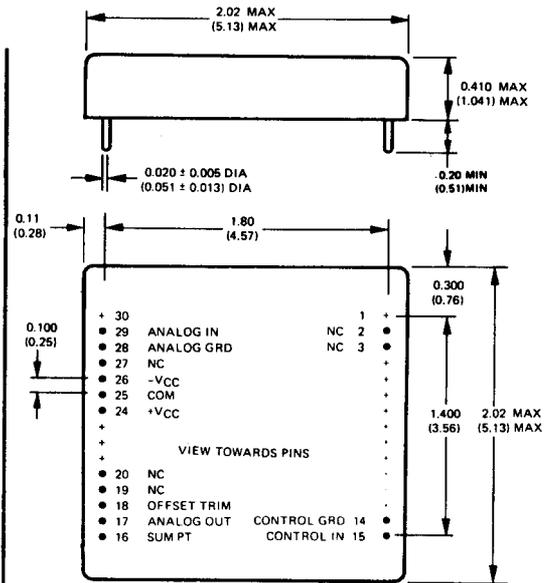
±0.01 Non-cumulative tolerance between pins
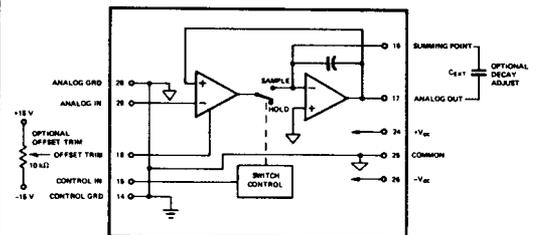±0.02 Tolerance from case edge to center of pins

DIMENSIONS IN PARENTHESES ARE EXPRESSED IN CENTIMETERS

Mechanical Specifications

Pin	Signal		Pin
30	ANALOG IN	NC	1
29	ANALOG GRD	NC	2
28	ANALOG GRD	NC	3
27	NC		
26	−VCC		
25	COM		
24	+VCC		
	VIEW TOWARDS PINS		
20	NC		
19	NC		
18	OFFSET TRIM		
17	ANALOG OUT	CONTROL GRD	14
16	SUM PT	CONTROL IN	15

BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.50 (1.27)

Optional Socket: Model 6069

NOTE: USE A CERMET POTENTIOMETER AND A POLYSTYRENE OR TEFLON CAPACITOR.

Model 4854 Block Diagram

Teledyne Philbrick makes no representation that use of its modules in the circuits described herein, or use of other technical information contained herein will not infringe on existing or future patent rights nor do the descriptions contained herein imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith.

TELEDYNE PHILBRICK

Allied Drive @ Rte. 128; Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439