TELEDYNE PHILBRICK

Modular High Speed Sample Hold Amplifier

4855

The 4855 High Speed Sample-Hold Amplifier was designed for use in high speed, multiplexed data acquisition systems requiring high accuracy and wide bandwidth. High throughputs for 12 bit systems are ensured by the 4855's ability to acquire a 10V signal to an accuracy of ± 1mV in 250nsec. Sample to hold settling time (also to ± 1mV) is an extremely low 100nsec maximum. When the 4855 is used with Teledyne Philbrick's 4133 12 Bit A/D Converter, system throughputs higher than 375kHz are achievable.

The 4855's high input impedance ($10^{11}\Omega$) and its high feedthrough attenuation make it an excellent choice for multiplexed systems. Feedthrough in the hold mode is guaranteed less than 1mVp-p for a 20Vp-p 1MHz input. This makes higher system throughputs possible in that system input channels can be overlapped, i.e., the input multiplexer can be switched and allowed to settle into a new channel while the A/D converter is still converting a previously held input signal from a different channel. The 4855 has a 2MHz full power bandwidth and special circuitry has been employed to minimize phase shift and amplitude errors at high frequencies.

Offset Voltage Trim

The offset voltage in either the sample or hold mode may be trimmed to zero while cycling between sample and hold with the input grounded by adjusting the 10kΩ potentiometer (shown in Figure 1) for zero volts output. This procedure does not reduce the pedestal—the unwanted DC step in output voltage that occurs as one switches from sample to hold.

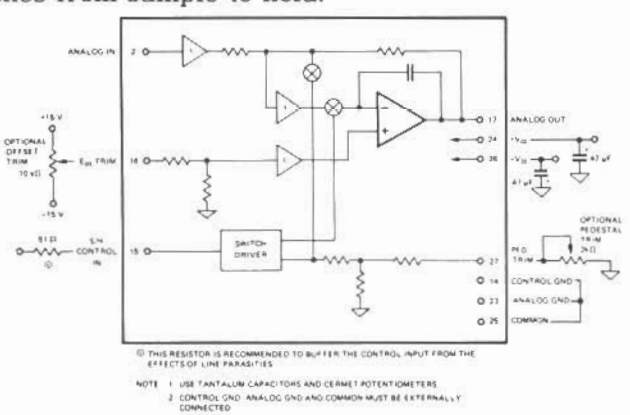
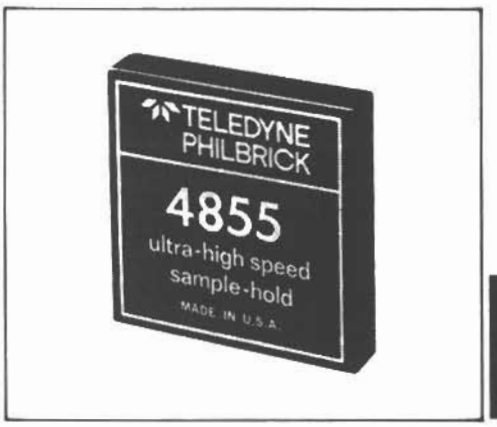


Figure 1. Functional Block Diagram



FEATURES

- 250nsec Acquisition Time
- 100nsec Settling Time
- ±200psec Aperture Uncertainty
- ±0.005% Nonlinearity
- High Input Impedance
- Low Feedthrough

APPLICATIONS

- Data Acquisition Systems
- Fast Fourier Transforms
- Medical Scanning Equipment
- Radar Pulse Analysis

TELEDYNE PHILBRICK Allied Drive @ Rte..128, Dedham, Massachusetts 02026
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SPECIFICATIONS (At +25°C, ±15 V, unless otherwise indicated)

	TYPICAL	GUARANTEED
INPUTS		
Analog		
Voltage	±11V	±10V
Bias Current	±10pA	±50pA
Impedance	$10^{11}\Omega \parallel 2pF$	---
Power		
Voltage, $\pm V_{CC}$	---	±15V ±1%
Current (Quiescent)	±75mA	±90mA
Digital		
Sample Level	---	⩽+0.8V
Hold Level	---	⩾+2.0 V
Loading ①	---	1 TTL Load
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity	±0.003% of F.S.	±0.005% of F.S.
Gain (nominal at dc)	−1.000	---
Gain Error ②	±0.01%	±0.02%
Sample Voltage Offset ③⑧	±2mV	±5mV
Hold Voltage Offset ③④⑧	---	±12mV
Pedestal Voltage ③④⑧	±3mV	±7mV
Droop Rate in Hold ⑤	±5μV/μs	±25μV/μs
Feedthrough in Hold ⑥	---	1mV P-P
Stability		
Gain vs. Temp.	±15ppm/°C	---
Sample Voltage Offset vs. Temp.	±15μV/°C	±50μV/°C
Hold Voltage Offset vs. Temp.	±100μV/°C	---
PSRR	0.01% of F.S./%ΔV_{CC}	---
Long Term Stability	0.01%/year	---
Dynamic Characteristics		
Bandwidth		
−3dB See Fig. 3	6MHz	---
Full Power Sine	2MHz	---
Slew Rate	250V/μsec	150V/μsec
Aperture Delay Time ⑦	2nsec	5nsec
Aperture Time ⑦	1nsec	2nsec
Aperture Uncertainty Time ⑦	±0.2nsec	---
Acquisition Time		
(10V Step) to 0.01% F.S.	250nsec	300nsec
(10V Step) to 0.1% F.S.	175nsec	---
(20V Step) to 0.01% F.S.	400nsec	---
(20V Step) to 0.1% F.S.	220nsec	---
(20V Step) to 0.2% F.S.	180nsec	---
Sample to Hold Transient	100mV	---
Settling Time, Sample to Hold		
to 0.01% F.S.	80nsec	100nsec
to 0.1% F.S.	40nsec	---
Signal Delay (DC to 2MHz)	22.5nsec	---
OUTPUT		
Voltage	±11V	±10V
Current	±50mA	±40mA
Load Capacitance, max.	100pF	75pF
ENVIRONMENTAL SPECIFICATIONS		
Operating Temperature Range	---	0°C to +70°C
Storage Temperature Range	---	−55°C to +125°C
Relative Humidity	95% non-condensing	---
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage to Ground	---	±18V
Digital Input Voltage	---	+5.5V
Analog Input Voltage	---	±18V
Short Circuit Protection, Output to Ground	---	Indefinitely

① A standard TTL unit load is −1.6 mA max. at ⩽+0.8V and +40μA max. at ⩾+2.0V.
② For 10Hz, 20V P-P sine wave.
③ Trimmable to zero.
④ With 604Ω from Pin 27 to Ground
⑤ Rate doubles for every 10°C increase in temperature
⑥ For 1MHz, 20V P-P sine wave. See Figure 2.
⑦ To ensure maximum performance, SCHOTTKY Logic should be used. Max. control signal rise time of 10nsec.
⑧ Best trim conditions for Offset Voltages and Pedestal Voltage may not occur simultaneously.

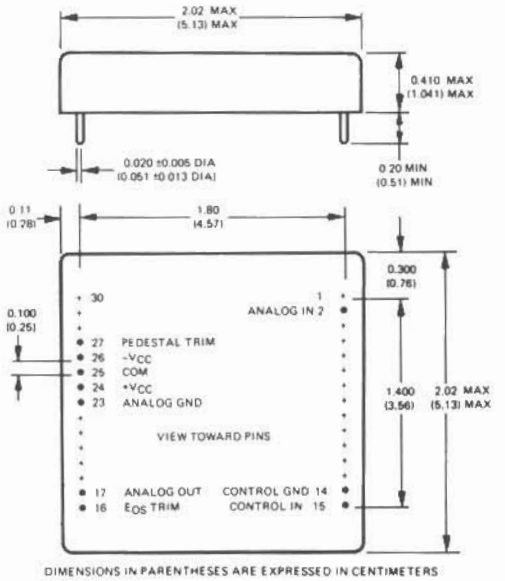
Pedestal Trim

The pedestal voltage, which is the difference between the sample offset voltage and the hold offset voltage, may be trimmed to 0 volts while cycling between sample and hold with 0 volts input and adjusting the 2kΩ potentiometer shown in Figure 1, for 0 volts difference. At least 10 minutes warm-up time before doing any trimming is recommended.

Power and Grounding Considerations

The ±15V inputs should be externally bypassed to ground with 47μF tantalum capacitors.

Control ground, analog ground and power supply common are not internally connected and must be externally connected to ensure that there are no ground loop errors.



Optional Socket: Model 6130
MECHANICAL SPECIFICATIONS

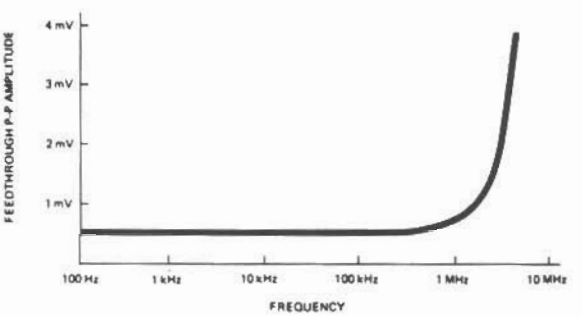


Figure 2. Feedthrough for 20 Volt P-P Sine Wave

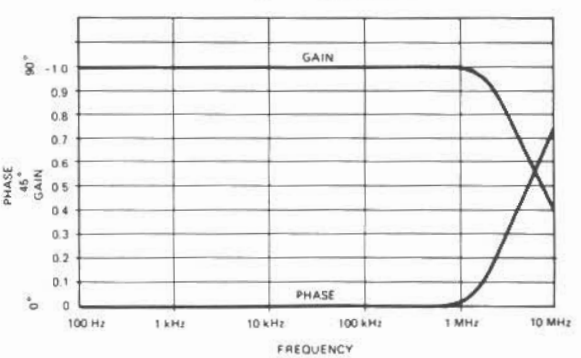


Figure 3. Gain/Phase vs. Frequency

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