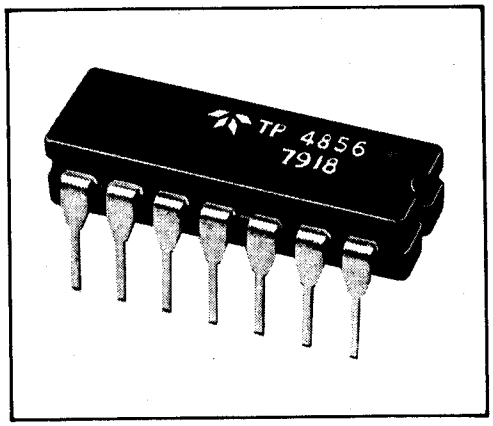
TELEDYNE PHILBRICK

Low Cost, Fast General Purpose Sample-Hold Amplifier

4856

The 4856 is an extremely versatile, high performance, monolithic sample-hold amplifier. This unit has been designed for maximum versatility in circuit design and "tailoring" of specifications. With a minimum of external components, the 4856 can be configured for inverting or noninverting applications with or without gain. In the sample mode, the 4856 acts as an op amp, and any of the standard op amp feedback circuits may be externally connected to control such parameters as gain and frequency response. In addition, the externally connected hold capacitor enables the user to achieve the best compromise between acquisition time and decay rate for different applications.



Applications Information

The offset voltage in either the "sample" or "hold" mode may be trimmed to 0 volts while cycling between sample and hold with 0 volts input and adjusting the 100kΩ potentiometer, shown in Figure 2, for 0 volts output. This procedure does not reduce the difference between the sample and hold offset voltages. At least 10 minutes warm-up time before trimming is recommended. The droop rate for the 4856 is determined by the value of the external capacitance, C_H, shown in Figure 2. The curves in Figure 1 give the value of C_H for the desired droop rate, as well as the effect on acquisition time. It is important to choose a polystyrene, mica, or teflon capacitor for the external connection to minimize errors caused by dielectric absorption. Also, to reduce the effects of stray inductance, the external capacitor should be located close to the unit. For minimum droop rate during hold, leakage paths on the p.c. board and on the package surface must be minimized. The output line can be used to form a guard ring around the hold capacitance pin. Because of the very nearly equal potentials between the output and the hold capacitance pin, the guard ring will result in a very low leakage current. In addition, pins 10 and 12, which are not internally connected, may be connected to the guard ring to reduce package surface leakage.

FEATURES

- 4μsec Acquisition Time
- Versatile—Inverting, Noninverting, With or Without Gain
- 10MΩ Input Resistance
- 2MHz Bandwidth
- ±0.005% Linearity
- 150mW Power Consumption

APPLICATIONS

- Data Acquisition Systems
- Analog Memories
- Data Distribution Systems
- Deglitch Circuits

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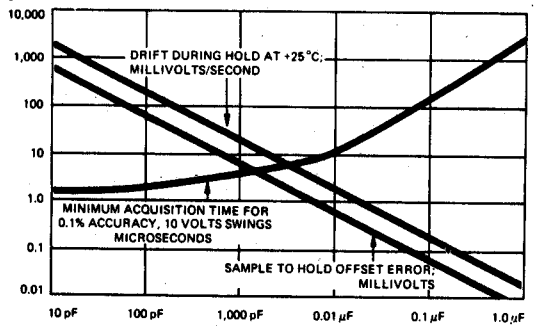
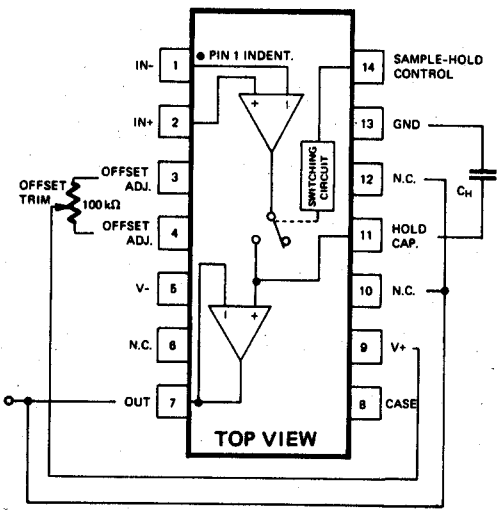
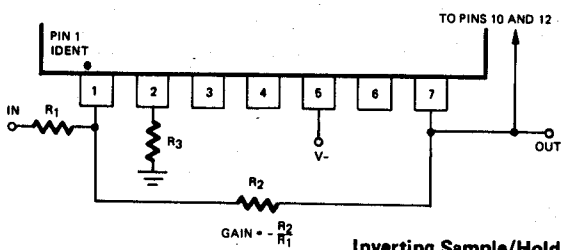


Figure 1. Typical Performance Curve

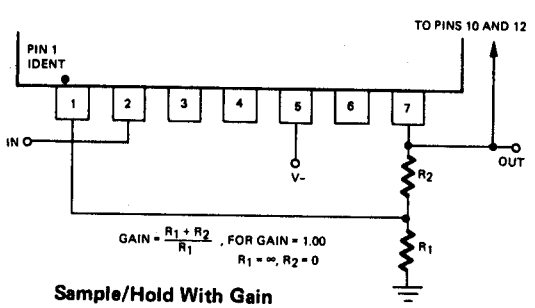


NOTES
1. USE CERMET POTENTIOMETER
2. C_H SHOULD BE A POLYSTYRENE, MICA, OR TEFLON CAPACITOR. THE VALUE OF C_H TO BE DETERMINED FROM FIGURE 1.

Figure 2. Block Diagram



Inverting Sample/Hold



Sample/Hold With Gain

Figure 3. Pin Programming

SPECIFICATIONS (At 25 °C, ±15 V, C_H = 1000 pF, unless otherwise indicated)

	4856 TYPICAL	GUARANTEED
INPUTS		
Analog		
Voltage	---	±10 V
Resistance	10 MΩ	5 MΩ
Bias Current, at 25 °C	50 nA	200 nA
Bias Current, Operating Temp. Range	---	400 nA
Power	---	±15 V @ ±5 mA
Recommended Philbrick Supply	2210	
Digital		
Sample Model Level, Operating Temp. Range	---	≤ 0.8 V at 0.8 mA max.
Hold Model Level, Operating Temp. Range	---	≥ 2.0 V at 20 μA max.
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity	0.005%	---
Large Signal Voltage Gain ①	50 K	25 K
Sample Offset Current, at 25 °C	10 nA	50 nA
Sample Offset Current, Operating Temp. Range	---	100 nA
Sample Offset Voltage, at 25 °C	3 mV	6 mV
Sample Offset Voltage, Operating Temp. Range	4 mV	8 mV
Charge Transfer ①	10 pC	20 pC
CMRR ①	90 dB	74 dB
Drift Current, at 25 °C ④	5 pA	50 pA
Drift Current, Operating Temp. Range	0.05 nA	1 nA
Stability		
Power Supply Rejection Ratio	90 dB	74 dB
Dynamic Characteristics		
Full Power Bandwidth ③ ⑤	70 kHz	---
Gain Bandwidth Product ①	2 MHz	---
Slew Rate ③ ⑤	5 V/μsec	---
Rise Time ⑥ ⑦	100 nsec	---
Overshoot ⑥ ⑦	20%	---
Aperture plus Aperture Delay Time	50 nsec	---
Aperture Uncertainty Time	7 nsec	---
Acquisition Time to 0.1% of F.S. ⑧ ⑨	4 μsec	---
0.01% of F.S.	5 μsec	---
OUTPUTS		
Voltage	---	±10 V
Current	---	±10 mA
Resistance	5 Ω	---
ENVIRONMENTAL SPECIFICATIONS		
Operating Temperature Range	---	0 °C to +75 °C
Storage Temperature Range	---	-65 °C to +150 °C
ABSOLUTE MAXIMUM RATINGS		
Voltage between V+ and V- pins	---	40 V
Differential Input Voltage	---	±30 V
Digital Input Voltage	---	+8 V, -15 V
Internal Power Dissipation ⑩	---	300 mW
Output Current	---	Short Circuit Protected

① R_L = 2 KΩ
③ Hold Jump Voltage (V) = Charge (pC)/C_H (pF)
⑤ V_{cm} = +5 Vdc
⑥ Decay Rate (ΔV/ΔT) = (pA)/C_H (pF)
⑦ A_V = +1, R_L = 2 KΩ, C_L = 50 pF
⑧ V_{out} = 20 V P-P
⑨ V_{out} = 400 mV P-P
⑧ V_{out} = 10 V P-P
⑨ C_H = 0.001 μF
⑩ Above +105 °C Ambient Temperature derate by 4.3 mW/°C

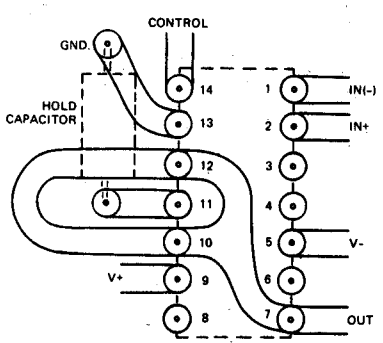
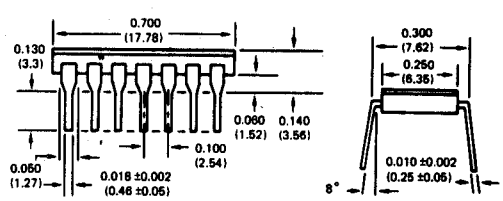


Figure 4. Guard Ring Layout (Bottom View)



14 LEAD PLASTIC DIP

Dimensions in Parentheses are Expressed in Millimeters.
All dimensions are ±0.01 (0.25) unless otherwise indicated

Figure 5. Mechanical Specifications

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