TELEDYNE PHILBRICK

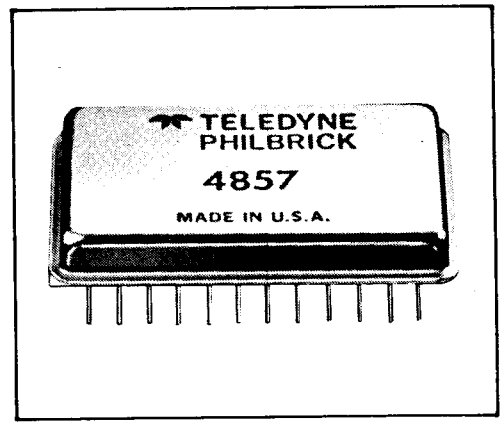
High Speed High Accuracy Sample-Hold Amplifier

4857

The 4857 is an extremely versatile, TTL compatible, dual-in-line packaged sample-hold amplifier that offers one of the best combinations of accuracy, stability, speed, and price available in a sample-hold today. For accuracy, the 4857 offers a maximum unadjusted gain error of ±0.02%, a maximum offset error of ±2mV, a maximum pedestal of ±3mV, and a maximum linearity error of ±0.002%FS (equivalent to ±0.001%FSR or ±½LSB for 15 bits). All four of these specifications are the best guaranteed by any hybrid manufacturer today, and they make the unadjusted 4857 adequate for 14 bit applications. For stability, the 4857 offers a gain drift guaranteed less than ±5ppm/°C, an offset drift less than ±100μV/°C, and a pedestal drift less than ±100μV/°C. For speed, the 4857 offers an acquisition time less than 1μsec (10V step to ±0.01%FS), an aperture delay time less than 32nsec, and an aperture jitter of ±100psec. Droop rate is an unequalled ±0.5μV/μsec max at +25°C and an outstanding ±100μV/μsec max at +125°C (4857-83). Feedthrough is an unequalled 80dB.

The 4857 is one of the few high resolution S/H's using the diode bridge switching technique. The bridge's low leakage current and a proprietary summing point compensation scheme help account for the 4857's low droop rate. The bridge's low capacitance and another compensation scheme are the reasons for the 4857's small pedestal. Pedestal, offset, gain and droop are all functionally laser trimmed at the factory for initial accuracy. If the guaranteed specifications are not adequate, the 4857 is externally adjustable for all four error sources, including droop rate.

The 4857 is packaged in a 24-pin, hermetically sealed dual-in-line package that also contains an uncommitted, high impedance ($10^{12}\Omega$) input buffer that can be configured as a follower, as a differential amplifier, or as a single ended amplifier with inverting or noninverting gain. For military/aerospace applications, the 4857 is available fully specified and tested for −55°C to +125°C operation and fully screened to the requirements of MIL-STD-883, Method 5008 (add "-83" to part number).



FEATURES

- 1μsec Max Acquisition Time
- ±100psec Aperture Jitter
- ±0.5μV/μsec Max Droop Rate
- 80dB Feedthrough Attenuation
- Optional Input Buffer
- 24 Pin Hermetic DIP
- −55°C to +125°C Operation
- MIL-STD-883 Screening

APPLICATIONS

- High Speed/High Accuracy Data Acquisition Systems
- Data Distribution Systems
- Deglitching Circuits
- Peak Detectors

TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($\pm V_{CC}$, Pins 18, 20)	± 18 Volts
Analog Input (Pin 9) (Note 1)	± 18 Volts
Analog Input (Pins 11, 12) (Note 1)	± 16 Volts
Differential Input (Pins 11, 12) (Note 1)	± 30 Volts
Digital Input (Pin 24)	± 18 Volts
Output Current (Note 2)	± 25 mA
Operating Temperature Range	− 55°C to + 125°C
Specified Temperature Range	
4857	0°C to + 70°C
4857-83 (Note 3)	− 55°C to + 125°C
Storage Temperature Range	− 65°C to + 150°C

SPECIFICATIONS (T_A = + 25°C, $\pm V_{CC}$ = ± 15V unless otherwise indicated)

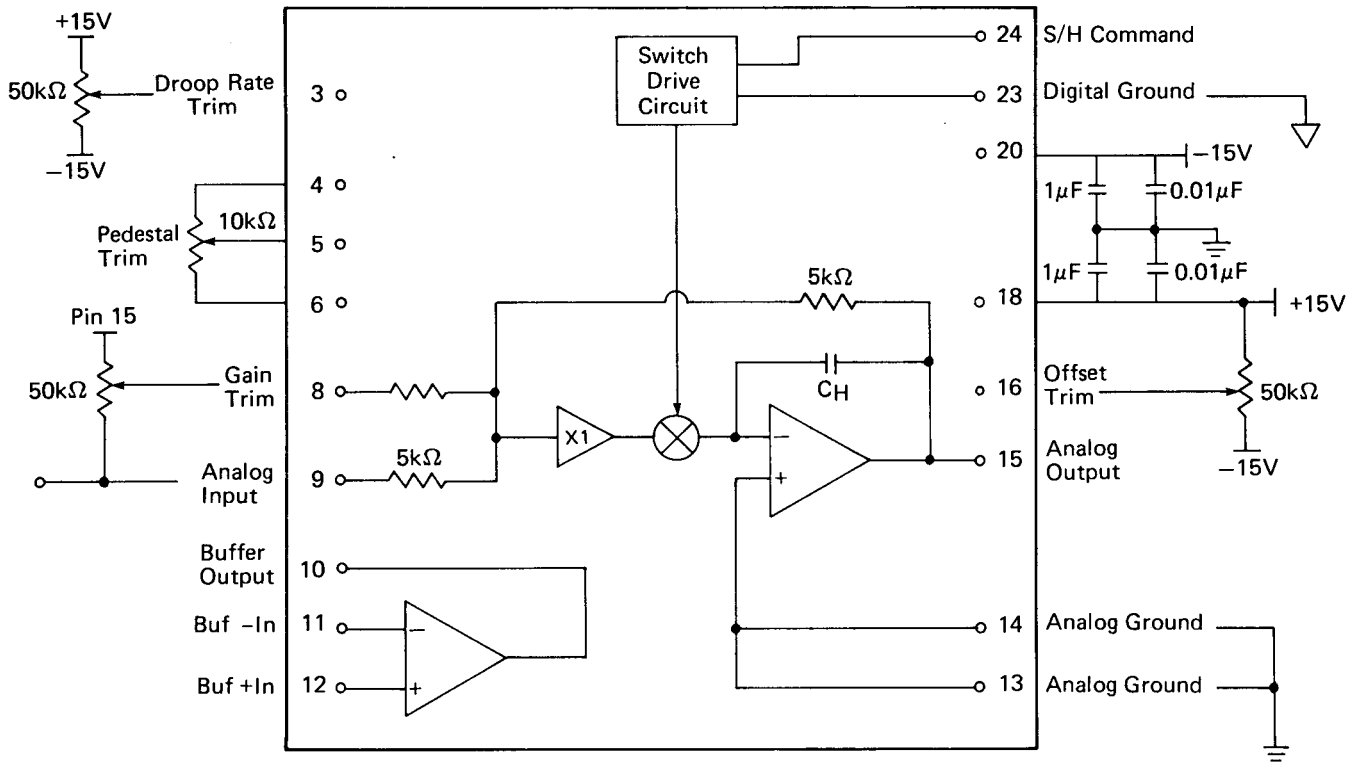
PARAMETER	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT/OUTPUT				
Buffered Input: Differential Voltage Range	± 10.25	± 11		Volts
Common Mode Voltage Range		± 11		Volts
Input Impedance		$10^{12} // 3$		Ω // pF
Input Bias Current		± 25	± 200	pA
Offset Voltage (Buffer Only)		± 3	± 12	mV
Offset Drift (Buffer Only)		± 5		μV/°C
CMRR (Buffer Only)		90		dB
Unbuffered Input: Voltage Range	± 10.25	± 11		Volts
Input Impedance		5		kΩ
Output Voltage Range	± 10.25	± 11		Volts
Output Current (Note 2)	± 7.5	± 20		mA
Output Impedance		0.2		Ω
Maximum Capacitive Load	200	1000		pF
DIGITAL INPUT				
Logic Levels: Logic "1" (hold mode)	+ 2.0		+ 5.5	Volts
Logic "0" (track mode)	0		+ 0.8	Volts
Loading		2kΩ to Ground		
TRANSFER CHARACTERISTICS (Note 4)				
Gain		− 1.00		V/V
Gain Accuracy (Note 5)		± 0.005	± 0.02	%
Gain Linearity Error: Buffered		± 0.008	± 0.02	%FS
Unbuffered		± 0.001	± 0.002	%FS
Offset Voltage (Sample Mode) (Note 5): 4857		± 1	± 5	mV
4857-83		± 1	± 2	mV
Pedestal (Notes 5, 6): 4857		± 1	± 5	mV
4857-83		± 0.5	± 3	mV
Stability: Gain Drift		± 1	± 5	ppm/°C
Offset Drift (Sample Mode)		± 50	± 100	μV/°C
Pedestal Drift		± 50	± 100	μV/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time (Note 7): 10V step to ± 0.01%FS (± 1mV)		0.8	1.0	μsec
10V step to ± 0.1%FS (± 10mV)		0.6		μsec
20V step to ± 0.02%FS (± 2mV)		1.1		μsec
20V step to ± 0.2%FS (± 20mV)		0.8		μsec
Settling Time, Sample to Hold (Note 8):				
to ± 0.01%FS (± 1mV)		300	500	nsec
to ± 0.1%FS (± 10mV)		150		nsec
Sample to Hold Transient		50	100	mVp-p
Aperture Delay Time			32	nsec
Aperture Jitter		± 0.1		nsec
Output Slew Rate	± 20	± 30		V/μsec
Small Signal Bandwidth (− 3dB): Buffered	5	6		MHz
Unbuffered	7	7.5		MHz
Droop Rate (Note 5), 4857: + 25°C		± 0.1	± 1	μV/μsec
+ 70°C		± 5		μV/μsec
4857-83: + 25°C		± 0.1	± 0.5	μV/μsec
+ 125°C		± 30	± 100	μV/μsec
Feedthrough (20kHz, 20Vp-p input)		1.5	2	mVp-p

PARAMETER	MIN.	TYP.	MAX.	UNITS
POWER SUPPLIES				
Voltage Range		± 3		%
Power Supply Rejection Ratio		± 0.005		%FSR/%Vs
Quiescent Current Drain		± 30	± 40	mA
Power Consumption		900	1200	mW

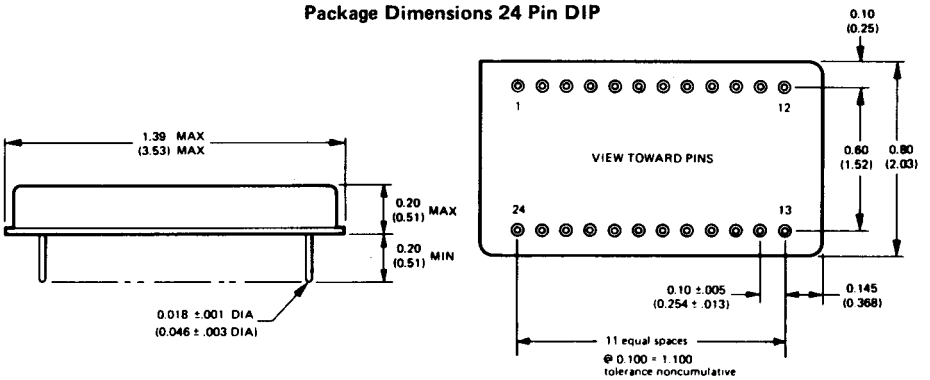
SPECIFICATION NOTES

1. Analog input signal should not exceed supply voltage. Buffer differential input should not exceed $+V_{CC} - (-V_{CC})$.
2. The 4857's S/H and buffer outputs can withstand sustained shorts to ground, but shorts to either supply will result in destruction.
3. The 4857-83 is specified for −55°C to +125°C operation and is processed and screened to the requirements of MIL-STD-883, Method 5008.
4. FS stands for Full Scale and is equivalent to 10 volts. FSR stands for Full Scale Range and is equivalent to 20 volts.
5. Gain accuracy, sample offset, pedestal and droop errors are adjustable to zero, at a given temperature, with external trim potentiometers.
6. Pedestal refers to the unwanted step in output voltage that occurs as a S/H is switched from its sample to hold mode. For many S/H's, pedestal amplitude is a function of input/output voltage level. For the 4857, the pedestal is constant regardless of input/output level.
7. Tested with $R_L = 1.33k\Omega$ and C_L less than 50pF. The 4857 has a full scale (FS) voltage of 10 volts and full scale range (FSR) of 20 volts. ± 1mV is equivalent to ± 0.01%FS or ± 0.005%FSR.
8. Sample to hold settling time refers to the time interval between the point at which a device is commanded from the sample to the hold mode and the point at which the analog output (following a transient) settles to within a specified error band around its final value.

Functional Block Diagram



Package Dimensions 24 Pin DIP

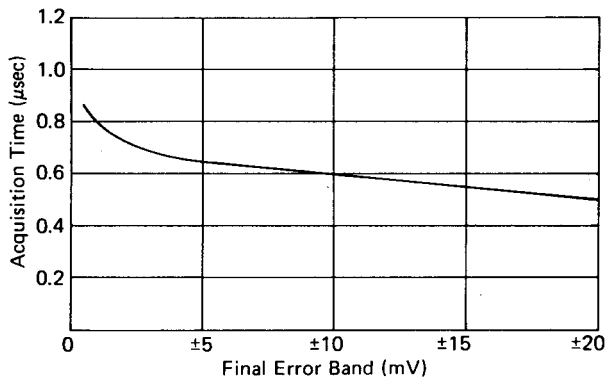


Dimensions are in inches (centimeters)

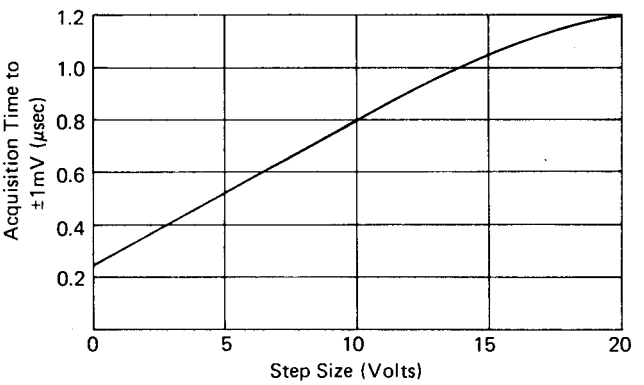
Pin Designations

1	N/C	24	S/H Command
2	N/C	23	Digital Ground
3	Droop Rate Trim	22	N/C
4	Pedestal Trim	21	N/C
5	Pedestal Trim	20	−15V Supply
6	Pedestal Trim	19	N/C
7	N/C	18	+15V Supply
8	Gain Trim	17	N/C
9	Analog Input	16	Offset Trim
10	Buffer Output	15	Analog Output
11	Buffer − In	14	Analog Ground
12	Buffer + In	13	Analog Ground

Acquisition Time vs. Final Error Band For a 10V Step



Acquistion Time vs. Input Step Size



Applications Information

Grounding and Bypassing

With proper grounding and bypassing, the 4857 will meet all its published performance specifications without additional external components. Pins 13 and 14 are both labeled analog ground. They should be tied together and both connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the 4857 and have pins 13 and 14 soldered directly to it. The 4857's metal package is grounded through pins 13 and 14, and a mylar insulator is supplied with each unit for isolation between case and pc board. Pin 23 (logic ground) is the reference point for the 4857's S/H command input (pin 24), and it can be connected to either system analog or system digital ground. If connected to analog ground, it should be soldered to the same ground plane to which pins 13 and 14 are soldered. Since the S/H command and digital ground go directly into a comparator (see Functional Block Diagram), high noise levels (−7V to +1.5V) can be present on the digital ground without a degradation in 4857 performance.

To achieve specified acquisition times, it is necessary to eliminate stray capacitance between the gain adjust point (pin 8) and ground either by using the gain trim potentiometer, by adding an external 0.1μF or larger capacitor between pin 8 and analog ground, or by actually cutting off the pin at the base plate. Small capacitances (2-10pF) between pin 8 and ground will introduce settling tails on the order of ±0.5mV/μsec.

For optimum performance and noise rejection, the 4857's ±15V supplies should each be bypassed to ground with one large capacitor (0.1μF tantalum or larger) in parallel with an 0.01μF ceramic capacitor. The capacitors should be located as close to the package as possible, as should the 4857's load, to minimize lead resistance and inductance.

Sample-Hold Command

A TTL logic "0" applied to pin 24 will put the 4857 into the sample (track) mode. In this mode (without the buffer), the device acts as an inverting unity gain amplifier, and its output will follow (track) its input. A logic "1" applied to pin 24 will put the 4857 into the hold mode, and the output will be held constant at the level present when the hold command was given. Pin 24 has an input resistance of 2kΩ to ground. With a logic "1" applied (+2.4V minimum), pin 24 will sink 1.2mA. Pin 24 should be driven by its own totel-pole-output, Schottky TTL circuit, such as a 74S132.

Capacitive and Resistive Loading

To avoid possible oscillation, current limiting, and performance variations over temperature, the 4857's output loading has certain restrictions. The maximum capacitive load guaranteed to avoid oscillation is 200pF, though units can typically drive >1000pF without problems. The 4857's output is short-circuit protected to ground with current limiting at approximately ±25mA. Recommended resistive loading is less than 1.33kΩ (i.e., resistance >1.33kΩ) though typically loads as high as 500Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by load resistance greater than 1.33kΩ and load capacitance less than 50pF. Higher capacitances will affect both acquisition and settling time.

Accuracy Trimming

The 4857 will meet all published performance specifications without additional components and adjustments. For applications demanding the highest accuracies, optional adjusting procedures are described below. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature.

Offset Trim—Offset error in either the sample or hold mode can be trimmed to zero with a 50kΩ potentiometer between $\pm V_{CC}$ with its wiper tied to pin 16 (see Block Diagram) while observing the S/H output on an oscilloscope. With the input grounded, the sample offset can be trimmed in the sample mode. Hold offset has to be trimmed while cycling between sample and hold. The latter procedure does not reduce pedestal but can be used to compensate for it if sample offset is not important.

Pedestal Trim—Pedestal refers to the unwanted step in output voltage that occurs as a S/H is switched from the sample to the hold mode. Pedestal can be trimmed to zero with a 10kΩ potentiometer between pins 4 and 6 with its wiper tied to pin 5 (see Block Diagram) while observing the S/H output on an oscilloscope. Make the adjustment with the input grounded while cycling from sample to hold. This procedure does not affect sample offset, but it can be used to compensate for it, i.e., it can be used to reduce hold offset to zero while not affecting sample offset.

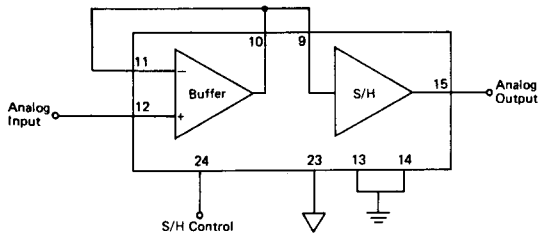
Gain Trim—When higher than ±0.02% gain accuracies are required, a 50kΩ potentiometer can be placed between the analog input and output (with or without the buffer) with the wiper tied to pin 8 (see Block Diagram). Gain must be trimmed with a nonzero input in the sample mode.

Droop Rate Trim—At a given temperature, output droop can be trimmed to zero with a 50kΩ potentiometer between $\pm V_{CC}$ and pin 3 (see Block Diagram). The adjustment should be made while cycling between sample and hold with a fixed input voltage and observing the S/H output with an oscilloscope.

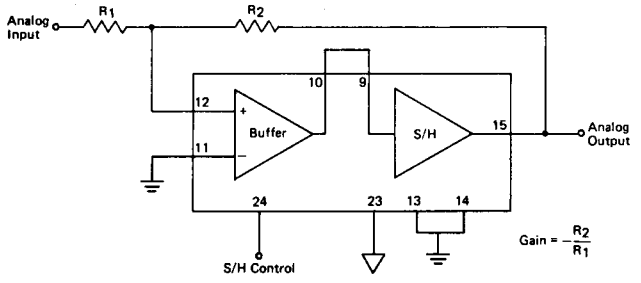
User-Optional Input Buffer

The 4857 contains a user optional, high performance input buffer. This is a FET input device with its inverting input (pin 11), noninverting input (pin 12), and analog output (pin 10) all brought out to package pins for greater flexibility. The amplifier used (LF356) was chosen for its high input impedance, low bias current, low offset voltage, and fast settling time. As described below, the buffer can be configured as a follower, as an inverting amplifier with gain, as a noninverting amplifier with gain, or it can be used for external services independent of the 4857's S/H function. Because of the op amp's uncommitted nature, any of the many schemes for optimizing op amp time and/or frequency response can be employed.

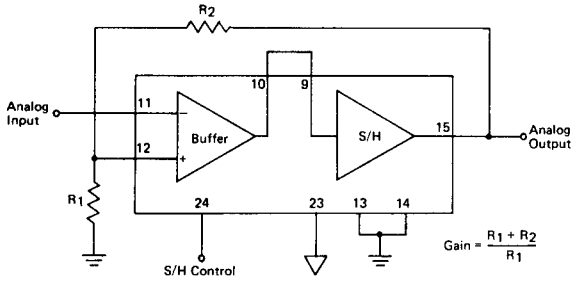
Follower—To use the 4857's internal buffer in a noninverting unity-gain configuration, tie pins 9, 10, and 11 together as illustrated at the top of the next page. With a DC input, acquisition time of the 4857 will still be below 1μsec. The buffer settling time (10V step settling to ±1mV) is approximately 2μsec, and this time should be added to the acquisition time if the 4857 is commanded to the acquisition mode with a rapidly changing buffer input.



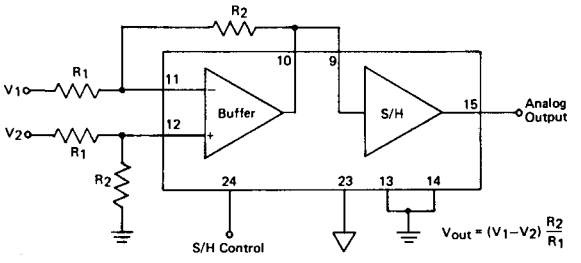
Inverting Amplifier—To use the 4857's internal buffer to attain overall S/H inverting operation with or without gain, connect it as shown below. By effectively placing the S/H in the feedback loop of the buffer amp, the effects of the buffer's output impedance and the S/H's offset error are greatly reduced. The S/H's optional offset adjust is ineffective in this configuration. Sample offset at the output will be that due to the buffer multiplied by the gain. With $R_1 = R_2$, acquisition time is typically 1.5μsec.



Noninverting Amplifier—To use the 4857's internal buffer to attain overall S/H noninverting operation, connect it as shown below. The optional offset adjust is ineffective in this configuration. Sample offset at the output will be that due to the buffer multiplied by the gain. If necessary, offsetting can be injected at the ground end of R_1.



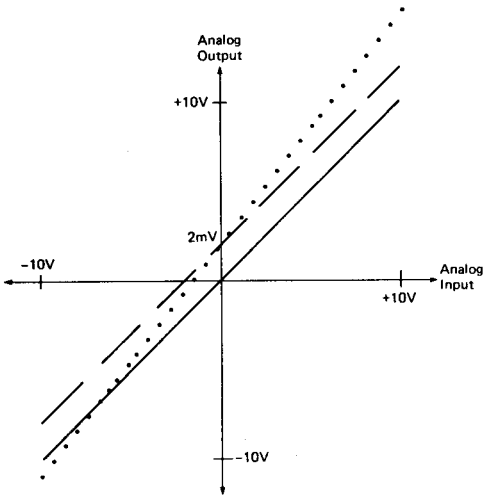
Other Configurations—Because of its uncommitted nature, the 4857's internal buffer can be used for any of the normal op amp functions independent of the unit's S/H function. In the diagram below, the buffer amp is configured as a differential amplifier. The 4857's offset trim works in this configuration. Sample offset at the 4857 output will be the sum of the errors due to the buffer and the S/H.



S/H Static Accuracy Errors

S/H amplifiers exhibit a number of static accuracy errors. The term "static" refers to the fact that these errors can be measured and tested with DC inputs as opposed to dynamic accuracy errors which require a changing analog input signal to become visible. Dynamic accuracy errors are discussed in the Teledyne Philbrick 4860 (200nsec 12 bit S/H amplifier) data sheet. The following explanations are slightly more applicable to track-hold amplifiers than to bonafide sample-hold amplifiers. All Teledyne Philbrick S/H amplifiers are really T/H amplifiers in that they can remain indefinitely in either the track or hold mode. A true S/H amplifier cannot track an input signal. When commanded to the sample mode, it takes a quick sample of the input signal and immediately returns to the hold mode. Most people use the terms S/H and T/H interchangeably with no resulting confusion.

Most T/H and S/H amplifiers have gains of + 1 or − 1. In the track (sample) mode, they look like unity gain amplifiers or unity gain inverters, and they exhibit the usual offset and gain errors we've come to expect from such devices. In the hold mode, they exhibit additional inaccuracies that are theirs alone. The solid line in the sketch at the top of the next page is the theoretical track-mode transfer function of a S/H with a gain of + 1 and a ± 10V input/output range. Its output equals its input. Linearity error (also called gain linearity error or simply, nonlinearity) describes the deviation between the actual transfer function and a reference straight line drawn through



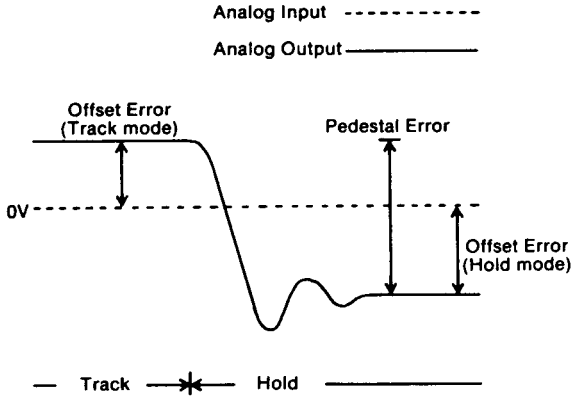
it. The reference line can be drawn to either a best-fit or an end-point criterion. Since linearity errors are usually orders of magnitude smaller than offset and gain errors, they make an almost negligible contribution to overall device accuracy (inaccuracy). They are obviously important, however, for system linearity requirements.

Tracking mode offset (also called track offset, sample offset or simply, offset) refers to the DC voltage appearing at the device output in the track (sample) mode with the analog input grounded. The units for track mode offset are usually mV, %FS or %FSR. Track mode offset behaves like any other offset in that it results in a constant voltage (the offset voltage) being added to every output level. Graphically, it results in a parallel displacement of the transfer function along the output axis. The broken line in the sketch is the transfer function of a S/H with a + 2mV track mode offset error and no gain error. Track mode offset is usually temperature dependent, and the drift can be specified in μV/°C, ppm's of FS/°C or ppm's of FSR/°C.

Gain error describes the difference between the actual and ideal values of the slope of the device transfer function. Gain error is usually measured and specified in the sample mode. Graphically, it results in a positive or negative rotation of the S/H transfer function around the zero point and hence results in input/output accuracy errors that are proportional to signal level. Gain error is normally expressed as a % (of ideal gain), and gain drift vs. temperature is normally expressed in ppm's/°C. In the sketch, the dotted line transfer function has a track mode offset error of + 2mV and a gain error of + 0.05%. Positive gain error has rotated the transfer function counterclockwise and increased its slope to a value greater than + 1. With a + 10V input signal, this device's tracking output will be + 10.007V. With a - 10V input signal, its output will be - 10.003V.

Pedestal, a specification unique to S/H amps, refers to the unwanted step in output voltage that occurs as a S/H is switched from the sample (track) mode to the hold mode. Units are usually the same as those for offset error. For most high resolution S/H's (those with linearity specs better than ± 0.01%FSR), the design approach is usually such that the pedestal will be the same sign and amplitude independent of input/output signal level. For many lower resolution devices, pedestal amplitude is a function of input/output signal level, and this dependence should be specified. Though pedestal can be measured at any input/output voltage level, it is normally measured with the input grounded, and it is normally measured by observing the S/H output on a scope while continually switching the unit from sample to hold. This procedure eliminates any measurement ambiguities resulting from output droop. Graphically, pedestal displaces the transfer function along the output axis and is equivalent to adding another offset. If the device with the dotted line transfer function had a + 3mV pedestal, its output error with a + 10V input would be + 10mV. At zero input, its output error would be + 5mV. At - 10V input, its output error, by coincidence, would be 0mV.

Hold mode offset is the DC voltage appearing at the output immediately after a S/H is commanded to the hold mode with the input grounded. As shown below, hold mode offset will be equal to the sum of track mode offset and pedestal. If pedestal is a function of signal level, it not only displaces the transfer function along the output axis, it changes its slope and is equivalent to adding both an offset and a gain error. In summary, a S/H amplifier with a nonzero input voltage can have an output error equal to the sum of its offset, gain and pedestal errors and still be within spec.

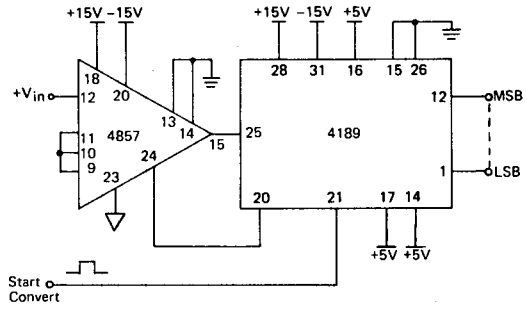


Using the 4857 with A/D Converters

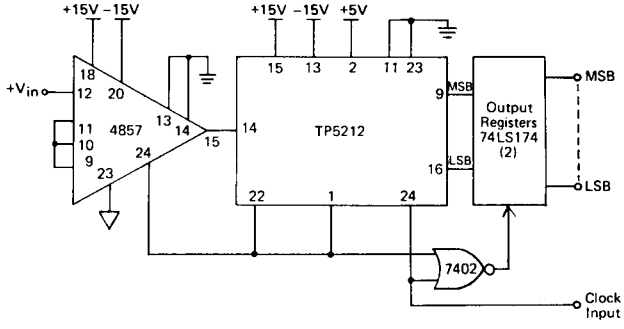
The most common use of a sample(track)-hold amplifier is ahead of an A/D converter to allow the digitizing of signals with slew rates (frequencies) much higher than the A/D alone can handle. A standard rule of thumb for ensuring accuracy in successive approximation type A/D conversion is that the input signal may not change by more than ± ½LSB during the conversion time. From this rule, it follows that a 12 bit (± ½LSB = ± 0.012%FSR) 5μsec A/D converter (like the Teledyne Philbrick 4189) cannot accurately digitize a ± 10V sine wave with a frequency above 7.8Hz. Placing a S/H amplifier with adequate track mode bandwidth in front of the A/D changes the rule of thumb limit. Now, the input signal may not change by more than ± ½LSB during the S/H's aperture jitter time. The 4857's ± 100psec aperture jitter permits the accurate 12 bit digitizing of ± 10V sine waves with bandwidths up to 194kHz—a considerable improvement. Needless to say, the S/H's output droop rate must be low enough to not allow the A/D's input to change by more than ± ½LSB during the A/D conversion time. See the data sheet for the Teledyne Philbrick 4860 (200nsec S/H) for an expanded discussion of aperture jitter and sample-to-hold settling time.

Two other considerations when using S/H's to drive successive approximation A/D's are that the S/H's output stage should exhibit very low impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock rate, and the S/H should be able to recover from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the S/H will be required to sink or source large high frequency current transients and recover within one clock period. In the hold mode, the 4857's output impedance is typically 0.2Ω. Its output typically recovers (to ± 0.01%) from a 2mA step in less than 300nsec.

In most applications using the 4857 in front of a successive approximation A/D converter, the 4857's S/H command pin can be driven directly (or inverted if necessary) from the converter's status output. The status output changes state when the converter receives a convert command, and this change can drive the S/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the S/H back into the track mode. The diagram below illustrates a 4857 mated with a Teledyne Philbrick 4189 (12 bit 5μsec A/D) in this manner. Since the 4189's MSB output is not set to its final value until one clock period (approximately 500nsec) after a conversion begins, the 4857's sample-to-hold transient will be completely settled, and no extra precautions are necessary.



If the A/D is an internal-clock device and it has to make continuous conversions, it may be necessary to use a one-shot to generate the 4857's sample pulse (see 4860, 4189, and TPADC85 data sheets for more information on this approach). If the A/D is externally clocked, the one-shot may not be required. The diagram below shows a 4857 mated with a continuously converting TP5212 (12 bit 13μsec A/D). Because the TP5212 is externally clocked, its status output (pin 22) will go low for a full clock period (1μsec) between conversions. This is enough time for the 4857 to acquire a new signal, and it can therefore be driven directly by the TP5212's status output. For latching output data, the TP5212's status output can be NORed with its clock to produce the required delay. See the TP5210 Series data sheet for more details.



TELEDYNE PHILBRICK Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600, TWX: (710) 348-6726, Tlx: 92-4439