TELEDYNE PHILBRICK

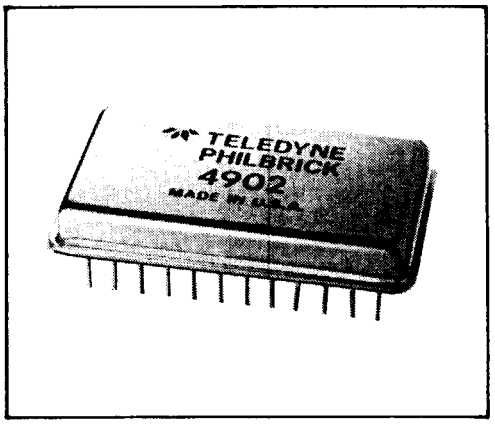
High Speed High Reliability Hybrid Deglitcher

4902

The 4902 high reliability hybrid deglitcher is designed to suppress transients at the output of digital to analog converters. These transients or glitches occur at the output whenever the DAC changes from one level to another. Minimizing glitches results in an ultra linear analog representation of a digital input. This is extremely important in applications such as CRT display driving where large high speed transients would be integrated over many microseconds causing distortion, affecting accuracy, and effectively lengthening system settling time by an order of magnitude. The deglitcher is a switched feedback element and therefore must be used in the feedback loop of a FET operational amplifier. The 4902 can be used with the 4058 DAC and 1430 op amp to make a high speed high reliability 12 bit deglitched DAC system with a maximum update rate of 1.66MHz.

The 4902's typical sample-to-hold and hold-to-sample glitch height is 8mVp-p (15mVp-p maximum) with a typical duration of 150nsec (200nsec maximum). Offset voltage is typically ± 5mV. Pedestal is ± 5mV maximum. The 4902 is specified for 0°C to + 70°C operation. For military/aerospace applications, the 4902-83 is fully specified for − 55°C to + 125°C operation and screened to MIL-STD-883, Method 5008.

The 4902's 24 pin, welded, all-metal dual in line case is hermetically sealed. Welding, instead of solder sealing, insures there is no contamination from flux gases or solder particles. This results in increased reliability. The all metal package provides shielding from EMI/RFI interference, thus enhancing feedthrough isolation.



FEATURES

- Glitch Characteristics
  Amplitude 15mVp-p Max
  Duration 200nsec Max
- Mates Directly With TP
  4058 High Speed DAC
  1430 FET Op Amp
- Can Be Used With Most High Speed DAC's
- 24 Pin Package
- − 55°C to + 125°C Operation
- Optional Screening to MIL-STD-883, Method 5008

APPLICATIONS

- CRT Display Systems
- Electron Beam Lithography Systems
- CRT Photo Typesetting
- Symbol Recognition and Analysis
- Ramp or Vector Generation
- Process Control
- Automatic Test Equipment

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THEORY OF OPERATION

Figure 1 shows the simplified block diagram of a sophisticated design concept. Combining a fast settling FET op amp, such as Philbrick's 1430, with the 4902 produces an extremely effective high-speed de-glitching circuit. This circuit uses the integration method to achieve precision performance and fast switching speeds. Fast switching action is accomplished by using a diode bridge with small voltage swings between ON and OFF states. The mode is controlled by steering the current through the proper set of diodes. The current is supplied by two current sources; the sum of which equals the amount of current going into the current sink. The diode bridge switches the hold capacitor in the feedback loop of the external operational amplifier. The control switch operates at ground potential, minimizing aperture uncertainty and leakage currents.

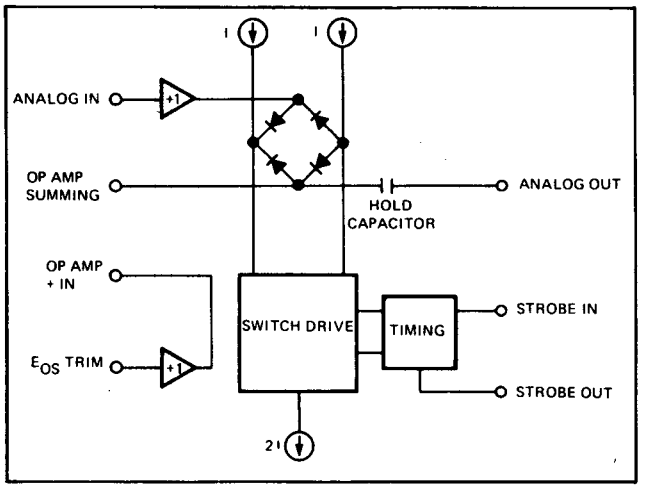


Figure 1. Simplified Block Diagram

TIMING AND WAVEFORMS

With external storage registers full, a strobe pulse, Strobe In, is applied to the deglitcher (see Figure 2). The rising edge of the Strobe In pulse places the deglitcher into the hold mode and triggers an internal "one shot" generating a gate pulse, Deglitcher Mode Control. Seventy nsec after the leading edge of the Strobe In pulse, the timing circuitry generates another gate pulse, Strobe Out, which strobes the parallel data from the registers to update the DAC. After the DAC has settled out, the falling edge of the Deglitcher Mode Control places the 4902 back into the sample mode, thereby reconnecting the DAC output to the amplifier, which quickly slews to its new value.

TRIM PROCEDURES

When greater accuracy is required, offset voltage (Eos) and hold jump voltage (pedestal) may be trimmed with external potentiometers as illustrated in Figure 3. Both OFFSET and JUMP potentiometers should be multi-turn, low temp-co cermet types. At least 10 minutes warm-up time before trimming is recommended.

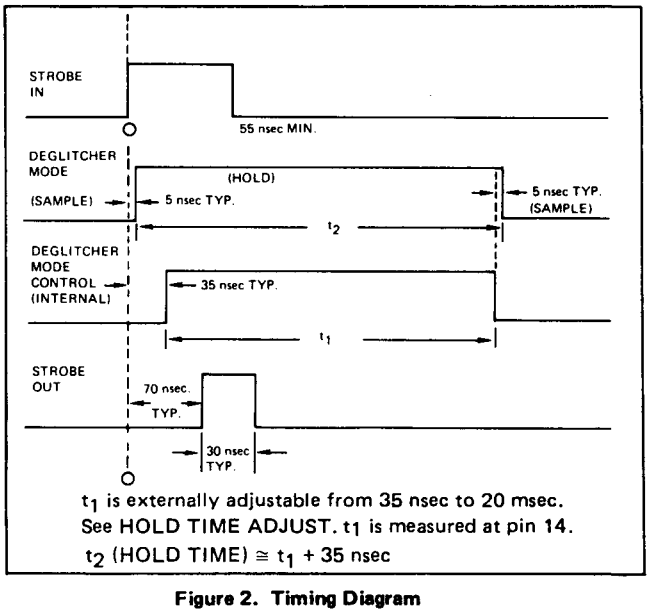


Figure 2. Timing Diagram

Offset Voltage Trim

The offset voltage in either the hold or sample mode may be trimmed to 0 volts while cycling between sample and hold with 0 volts input and adjusting the 10 kΩ potentiometer, shown in Figure 3, for 0 volts output. The trim range is approximately ±270 mV referred to output. This procedure does not, however, eliminate the difference between sample and hold offset voltages.

Hold Jump Voltage Trim

The hold jump voltage may be trimmed to 0 volts while cycling between sample and hold with 0 volts input and adjusting the 10 kΩ potentiometer shown in Figure 3, for 0 volts difference. The trim range is approximately ±10 mV referred to output.

Hold Time Adjustment

The deglitcher mode control circuit produces a pulse at its output in response to a trigger signal at its input. It is non-retriggerable, thus input triggers are ignored during the output cycle. The output pulse width is determined by an RC network. This circuit has an internal 22 pf capacitor, but a resistor must be externally connected as shown in Figure 3. Pulse width is adjustable from 35 nsec to 20 msec.

Since the mode control circuit is not retriggerable, the charge cycle time determines the output pulse width. The timing equation is (see Figure 2):

$$t_1 = RC \log_e 2 = 0.69\ RC \quad \text{where} \quad C = (22\ pf + C_{ext})$$

The resistor values should be between 1.4K–30KΩ. For precise pulse width applications a potentiometer should be used to set the output pulse width to the desired value. When longer output pulse widths are required, the 22 pf capacitance may be increased by adding a capacitor between pins 13 and 14 of the 4902. The maximum value of the external capacitance is 1 μf.

The total hold time (t_2) is determined by adding the delay time between the leading edge of the Strobe In pulse and the leading edge of the Deglitcher Mode Control pulse to the width of the Deglitcher Mode Control pulse (see Figure 2).

$$t_2 = t_1 + \text{delay}$$

This delay is typically 35 nsec with a maximum delay of 55 nsec. The Deglitcher Mode Control pulse is measured at pin 14.

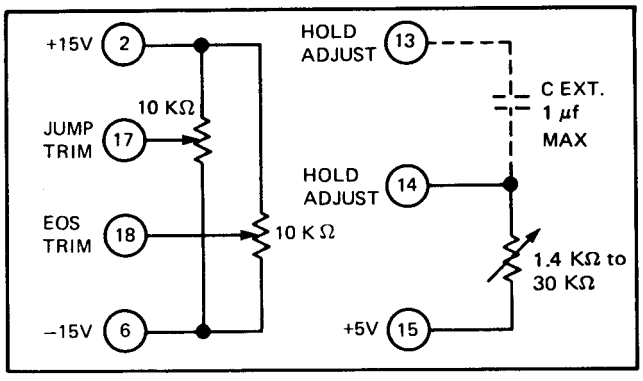


Figure 3. Trim Procedures

POWER AND GROUNDING CONSIDERATIONS

Power supplies of ±15V and +5 VDC are required. High speed systems require added care in power distribution for maximum accuracy and speed. The ±15V power supply inputs are internally bypassed on the 4902 with 0.33 μf ceramic capacitors to provide high frequency power supply decoupling. For optimized performance, it is recommended that all power supply input pins be bypassed to ground with 1 μf tantalum capacitors located as close to the device as possible.

Analog ground, and digital ground are not internally connected and must be externally connected to protect against ground loop errors. It is recommended that this connection be made at only one point, on a ground plane, as close to the device as possible.

GLITCHES AND DEGLITCHING

Glitches are transient spikes that occur at the output of any DAC whenever its input code is changed. They are caused by the time skew of analog switches and digital drive signals. Skewing is a result of switch imperfection, such as, stored charge or gate to drain capacity, causing switches to turn off faster than they turn on, or vice versa. This is normally most pronounced for small changes around the MSB where all the logic inputs are changing (see Figure 4). The skew time of the digital drive circuitry can be REDUCED by loading all logic bits into a storage register before updating the DAC. However, it is practically impossible to insure that all turn-on phenomena will coincide exactly with all turn-off phenomena for all code changes. *Even with the use of a deglitcher, glitches can never be completely eliminated.* The deglitching circuit isolates a DAC glitch from the output and substitutes its own small glitch. This glitch comes from charge-dumping on the deglitcher hold capacitor during transitions from Sample to Hold and Hold to Sample. Because it is independent of the DAC, glitch size will not vary with changes in the digital input codes. Therefore the glitch is small and constant.

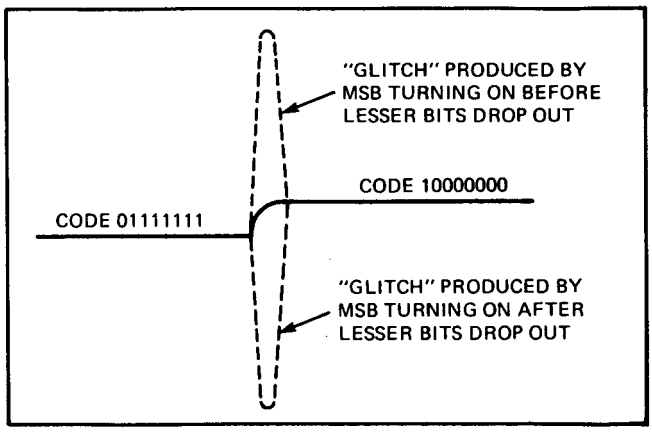


Figure 4. Glitch

Since a glitch is the result of charge dumping, its true measure is in coulombs or ampere-seconds. The deglitcher output signal is converted from current to voltage by the op amp. Therefore, in order to know the magnitude of the glitch, we must know its area. Given worst-case glitch amplitude in mV and duration in nsec, one can closely approximate area under the curve. Approximations are necessary due to the fact that glitches are not truly triangular in shape and the area under the curve will vary slightly from device to device.

Glitches are usually specified at a particular filtered bandwidth. System bandwidth affects the glitch, since its' amplitude may be reduced by filtering.

The 4902 is specified for a worst-cast peak-to-peak amplitude and duration at 5 MHz bandwidth. The duration is the time required from the start of the glitch until it settles to within ±1 mV. See Figure 5.

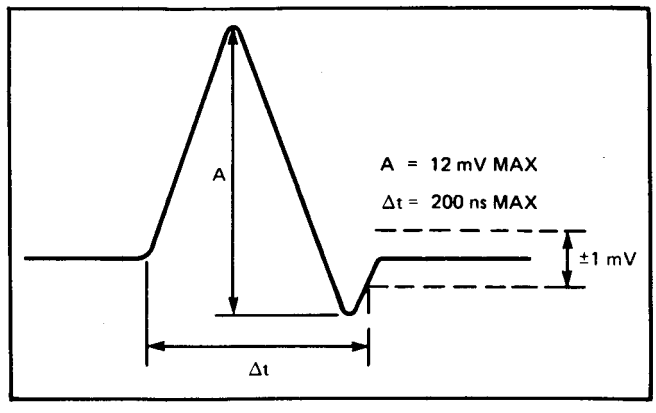


Figure 5. Measuring Glitch Characteristics of a Typical Glitch Waveform

DEGLITCHED DAC SYSTEMS

The 4902 can be used with just about any commercially available current DAC or FET input operational amplifier. However, it should be noted that the 4902 glitch characteristics are trimmed for use with a Teledyne Philbrick 1430 operational amplifier. Therefore, when operated with another amplifier, the glitch characteristics will change. Figure 6 shows a simplified block diagram of a deglitched DAC system.

Used With 4058 DAC and 1430 Op Amp

Figure 7 shows a detailed schematic of a deglitched DAC system employing the 4902, the 4058 high-speed, high-reliability 12 bit DAC, and the 1430 high-speed, high-reliability FET operational amplifier. In this system, resistors internal to the 4058 are employed as the feedback resistor shown in Figure 6. While the schematic shown in Figure 7 is for a system with ±5 volts output range other output ranges can be obtained with minor wiring changes as described in Table 1. A parts list is given in Table 2.

When used with the 4058, the hold pulse width should be at least 300 nsec. This insures that the deglitcher will not go into the sample mode before the 4058 has settled to within ±1/2 LSB. The hold pulse width may be adjusted to less than 300 nsec for applications requiring less than 12 bits accuracy.

Suggested Layout

A PC board (Model 6144) or PC board layout, detailed schematic and parts list is available, upon request, to assist our customers in achieving optimum deglitched DAC system performance. The system described utilizes Teledyne Philbrick's 4058 DAC and 1430 FET operational amplifier.

In Figure 7, the power supply bypass capacitors labeled C1, C2 and C3 are used to reduce power supply impedances at high frequency. Capacitor C4 is optional and is used for increasing the hold pulse width. C5 and R6 are used to prevent changes in the jump voltage over the range of TTL levels and rise times. CR1 and CR2 are back to back Schottky Barrier Diodes used to externally clamp DAC Input, pin 20.

To optimize settling time of the 4058 and to make the settling time independent of the characteristics of the driver, 2.2KΩ, 1/8 Watt pulldown resistors are recommended at all logic inputs. (See 4058 data sheet.)

Output Range	Jumper 4902 Pin 24 to 4058	4058 PIN PROGRAMMING		
		Jumper Pin 14 to	Jumper Pin 18 to	Jumper Pin 20 to
0 to −5V	Pin 19	Pin 15 ①	Pin 16	Pin 13
0 to −10V	Pin 19	Pin 15 ①	Pin 16	- - -
±2.5V	Pin 19	Pin 15 ①	Pin 24	Pin 13
±5V	Pin 19	Pin 15 ①	Pin 24	- - -
±10V	Pin 20	Pin 15 ①	Pin 24	Pin 15

① If oscillations or ringing occur, connect a 100kΩ resistor between Pin 14 and Pin 15.

Table 1. Range Programming

Circuit Symbol		Description	Part Number	
C1		Capacitors 6.8 μf	Sprague	150D685X9020 B
C2,C3		Capacitors 1 μf	Sprague	150D105X9020 A
C4		Capacitors 33 pf	AVX	CK12BX330K
C5		Capacitors 47 pf	AVX	CK12BX470K
CR1,CR2		Diodes 5082-2811	H.P.	5082-2811
R1,2		Resistors 1K 1/4W 10% CC	Allen-Bradley	Style RC
R3,R4,R5		Resistors, Variable	Bourns	3006P
R6		Resistors 200Ω	Allen-Bradley	Style RC
A1		DAC	TP	4058
A2		Deglitcher	TP	4902
A3		Amplifier	TP	1430
Z1, 2		IC's FF		74174

Table 2. Parts List for Deglitched DAC

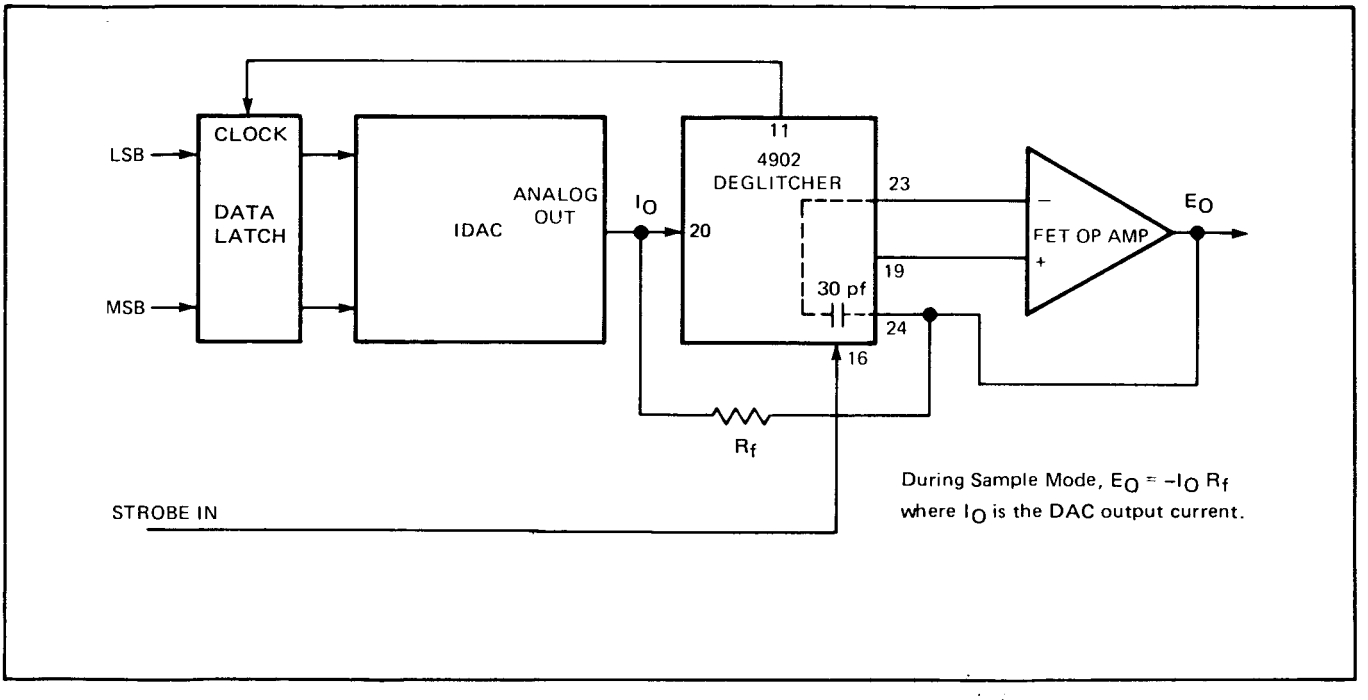


Figure 6. Simplified Block Diagram of Deglitched DAC System

4902 AS A SAMPLE-HOLD AMPLIFIER

The 4902 can be operated as a sample-hold amplifier by connecting a pair of tightly matched, low-TC metal film resistors as shown in Figure 8. This application provides a high speed, high reliability sample-hold amplifier with an operating temperature range of -25°C to +85°C. Figure 8 also shows some typical performance specifications.

Acquisition time of 1 μsec for a 10V step to 0.01% accuracy is an example of the exceptional stability and accuracy that recommends this circuit for use with fast 12 bit A/D converters.

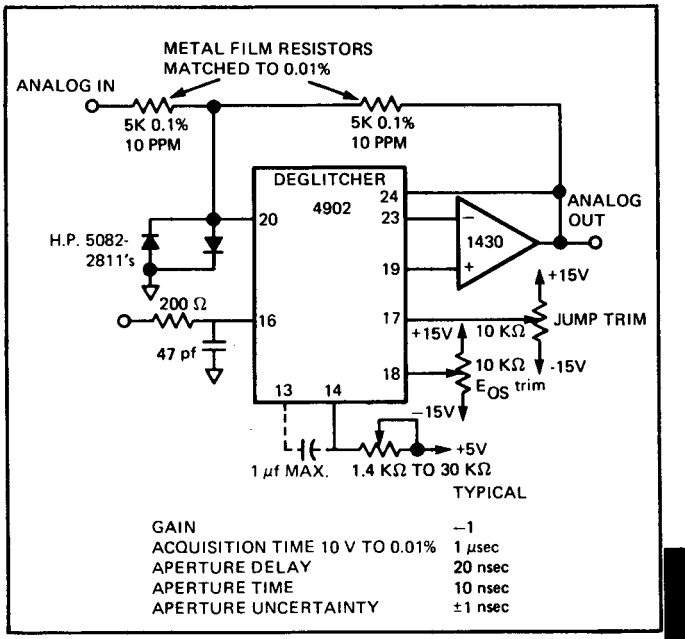
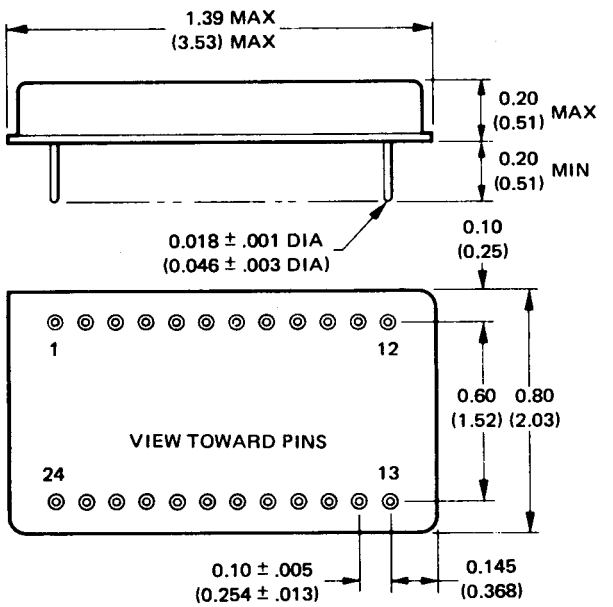


Figure 8. 4902 Operated as Sample-hold Amplifier



RECOMMENDED SOCKET: Augat Socket No. 324-AG2D or equivalent.

(Dimensions in parentheses are expressed in centimeters.)

PIN DESIGNATIONS

1. N.C.
2. +15V
3. N.C.
4. N.C.
5. N.C.
6. −15V
7. N.C.
8. ANALOG GROUND
9. N.C.
10. N.C.
11. STROBE OUT
12. DIGITAL GROUND
13. HOLD ADJUST
14. HOLD ADJUST
15. +5V
16. STROBE IN
17. JUMP TRIM
18. EOS TRIM
19. OP AMP (+ INPUT)
20. DAC INPUT
21. N.C.
22. N.C.
23. OP AMP (- INPUT)
24. DEGLITCHER OUTPUT

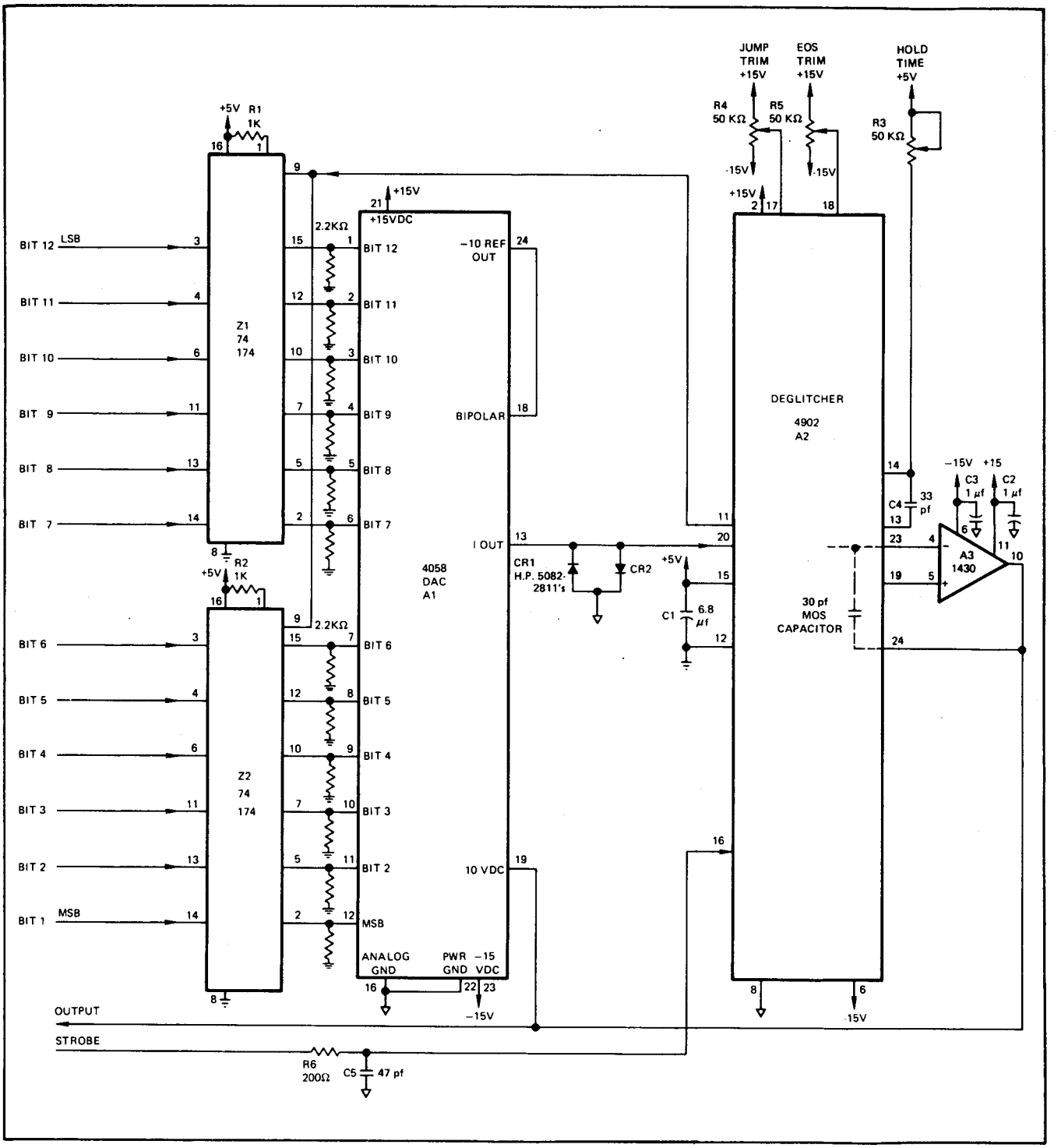


Figure 7. High Reliability Deglitched DAC System

NOTE: All power supply inputs of the individual components should be bypassed by a 10 μf tantalum capacitor in parallel with a 0.01 μf ceramic capacitor.

4902 SPECIFICATIONS @ +25°C, V_{CC} = ±15 V and +5 V, unless otherwise indicated

	TYPICAL	GUARANTEED
INPUTS		
Analog	---	①
Power		
Voltage	---	±15 V ±1%, +5 V ±1%
Current (Quiescent)	---	±25 mA, +80 mA
Recommended Philbrick Supply	2242	
Digital		
Strobe In		
Pulse Width min./max.	---	55 nsec/100 nsec
Rise Time ⑧	---	≤15 nsec
Fan In	---	2 TTL Loads
Strobe Out		
Pulse Width min./max.	30 nsec	15 nsec/50 nsec
Fan Out	---	10 TTL Loads
TRANSFER CHARACTERISTICS		
Accuracy		
Sample Offset Voltage ② ③ ⑦ ⑨	±5 mV	---
Hold Jump Voltage ② ③ ⑦	---	±5 mV
Decay Rate In Hold ⑦	---	25 μV/μsec
Feedthrough In Hold ⑦	---	±5 mV
Stability		
Sample Offset Voltage T.C. ⑦ ⑨	±25 μV/°C	---
Hold Jump Voltage T.C. ⑦	±30 μV/°C	---
PSRR (Non-tracking) ⑦	0.01% of F.S./%△V_{CC}	---
Dynamic Characteristics		
Sample/Hold and Hold/Sample Transients ④ ⑦	8 mV p-p	15 mV p-p
Sample/Hold and Hold/Sample Duration ⑤ ⑦	150 nsec	200 nsec
Aperture Time	100 nsec	---
OUTPUT		
Voltage ⑦	---	±10 V
Current ⑥ ⑦	---	50 mA
ENVIRONMENTAL SPECIFICATIONS		
Operating Temperature Range: Standard	---	0°C to +70°C
-83 Version	---	−55°C to +125°C
Storage Temperature Range	---	−65°C to +150°C
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage to Ground	---	±18 V, +6 V
Digital Input Voltage	---	+5.5 V
Analog Input Voltage	---	①
Short Circuit Protection, Output to Ground	---	Indefinite

① DAC Input, Pin 20, must be externally clamped with a pair of back to back Schottky Diodes connected between Pin 20 and Ground. (H.P. 5082-2811)
② Adjustable to zero.
③ The Hold Offset Voltage is the sum of the Sample Offset Voltage and the Hold Jump Voltage. All are adjustable to zero.
④ 5 MHz Bandwidth
⑤ 5 MHz Bandwidth at ±1 mV
⑥ R_{LL} = 200 Ω, E_O = 10 V
⑦ Using 1430 Output Op Amp
⑧ Use R.C. filter shown in Figure 7
⑨ At 10 V Full Scale

DEGLITCHED DAC SYSTEM (4902, 4058, and 1430) @ +25°C, V_{CC} = ±15 V and +5 V, unless otherwise indicated

	TYPICAL	GUARANTEED
RESOLUTION	———	12 Bits
TRANSFER CHARACTERISTICS		
Accuracy		
Nonlinearity at 25°C	———	±1/2 LSB
Nonlinearity –36°C to +125°C	±1/2 LSB	———
Differential Nonlinearity at 25°C	±1/4 LSB	±1/2 LSB
Differential Nonlinearity at –55°C	———	±2 LSB max.
Differential Nonlinearity from –36°C to +125°C	———	±1 LSB max.
Monotonicity	———	–36°C to +125°C
Sample Voltage Offset (adj.) ②	±5 mV	———
Sample Voltage Offset TC ②	±25 µV/°C	———
Hold Jump Voltage (adj.)	———	±5 mV
Hold Jump Voltage TC	±30 µV/°C	———
Gain Error	———	±0.05%
Gain Error TC	———	±7.5 ppm/°C
Dynamic Characteristics		
Acquisition time to 0.01% for:		
10 V Full Scale Step	600 nsec	1 µsec
10 LSB Step	250 nsec	400 nsec
1 LSB Step	200 nsec	300 nsec
Slew Rate	25 V/µsec	———
Decay Rate	———	25 µV/µsec
Glitch Characteristics	———	Glitch Amplitude: 15 mV max. Glitch Duration: 200 nsec
OUTPUTS		
Output Voltage	———	±10, ±5, ±2.5 0 to –5 V, 0 to –10 V
Output Current	———	50 mA
INPUTS		
Logic Code		
Unipolar	———	Binary
Bipolar	———	Offset Binary
Switching Levels	———	TTL
Power Supplies		
+15 VDC	———	+200 mA
–15 VDC	———	–200 mA
+5 VDC	———	+80 mA
TEMPERATURE SPECIFICATIONS		
Operating Temperature Range: Standard	———	0°C to +70°C
-83 Version ①	———	–55°C to +125°C
Storage Temperature Range	———	–65°C to +125°C

① 1430 needs heat sink above +85°C
② At 10 V Full Scale

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