

High Speed FET Input Operational Amplifier

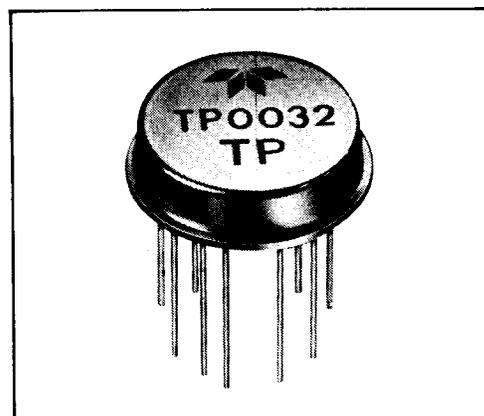
TP0032

The TP0032 is a high slew rate, FET input, fully differential operational amplifier. This device features a 70dB minimum open loop gain, a wide 80MHz bandwidth, high input impedance ($10^{11}\Omega$), and high output drive capabilities.

Although it can be used as a direct replacement for other LH0032 type op amps, the TP0032 features the following performance improvements:

1. Increased open loop gain improves linearity and eliminates output voltage droop.
2. Improved second stage biasing and decreased gain sensitivity to the transconductance of the JFET input yields faster and more consistent settling times.
3. The addition of bias compensation over temperature improves dynamic response vs. temperature.
4. Improved phase margin allows smaller compensation capacitance values to be used in low gain applications. This means that for new designs, the TP0032 will provide higher slew rates and faster settling times.

The standard TP0032 is specified for -55°C to $+125^{\circ}\text{C}$ operation. For high reliability military/aerospace applications, it is available with MIL-STD-883 screening (TP0032-83).

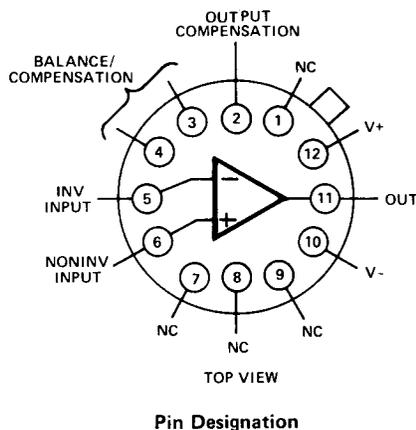


FEATURES

- Improved Second Source, Replaces All LH0032G
- 100ns Settling to $\pm 1\%$
- 650V/ μsec Slew Rate
- 70dB Min Open Loop Gain
- -55°C to $+125^{\circ}\text{C}$ Operation
MIL-STD-883 Screening

APPLICATIONS

- High Speed ADC Comparators
- ADC and SHA Integrators
- High Speed Integrators
- Video Amplifiers



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($\pm V_{CC}$)	± 18 Volts
Input Voltage	$\pm V_{CC}$
Differential Input Voltage	± 30 Volts
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$

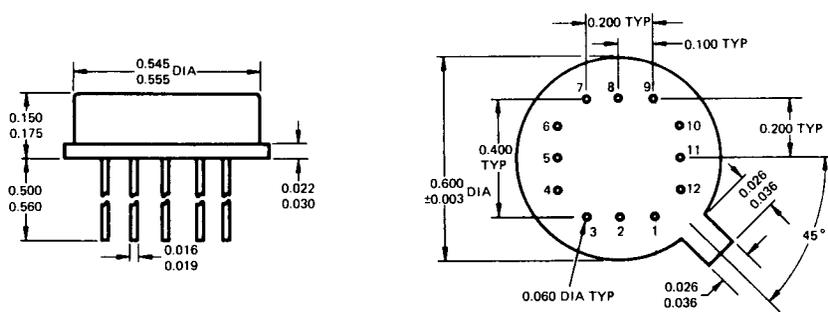
SPECIFICATIONS ($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $\pm V_{CC} = \pm 15\text{V}$ unless otherwise indicated)

PARAMETER	MIN.	TYP.	MAX.	UNITS
OPEN LOOP VOLTAGE GAIN ($R_L = 1\text{k}\Omega$):				
Initial ($T_A = +25^{\circ}\text{C}$)	70	85		dB
-55°C to $+125^{\circ}\text{C}$	70	83		dB
INPUT CHARACTERISTICS				
Differential Input Impedance		$10^{11} // 1.5$		$\Omega // \text{pF}$
Offset Voltage: Initial ($T_A = +25^{\circ}\text{C}$)		± 2	± 5	mV
-55°C to $+125^{\circ}\text{C}$		± 4	± 10	mV
Drift vs. Temperature		± 25		$\mu\text{V}/^{\circ}\text{C}$
Offset Current: Initial ($T_A = +25^{\circ}\text{C}$)		± 5	± 25	pA
-55°C to $+125^{\circ}\text{C}$		± 12	± 25	nA
Bias Current: Initial ($T_A = +25^{\circ}\text{C}$)		± 10	± 100	pA
-55°C to $+125^{\circ}\text{C}$		± 5	± 50	nA
Common Mode Voltage for DC Linear Operation	± 10	± 12		Volts
Power Supply Rejection Ratio ($\Delta V_{CC} = \pm 10\text{V}$)	50	70		dB
Common Mode Rejection Ratio ($\Delta V_{in} = 10\text{V}$)	50	70		dB
OUTPUT CHARACTERISTICS				
Voltage Swing ($R_L = 1\text{k}\Omega$)	± 10	± 13.5		Volts
Current (Note 1)	± 10	± 13.5		mA
FREQUENCY RESPONSE (Note 2)				
Unity-Gain Bandwidth (Note 3)		80		MHz
Slew Rate ($A_V = +1$, $\Delta V_{in} = 20\text{V}$)	350	650		$\text{V}/\mu\text{sec}$
Settling Time ($A_V = -1$)				
20V Step to within $\pm 1\%$		100		nsec
20V Step to within $\pm 0.1\%$		300		nsec
Small Signal Rise Time ($A_V = +1$, $\Delta V_{in} = 1\text{V}$)		8	20	nsec
Small Signal Delay Time ($A_V = +1$, $\Delta V_{in} = 1\text{V}$)		10	25	nsec
POWER REQUIREMENTS				
Quiescent Current ($T_A = +25^{\circ}\text{C}$)		± 17	± 20	mA

SPECIFICATION NOTES

1. The TP0032 is not output short circuit protected and neither are other vendors' 0032's.
2. Frequency Response specifications apply for $T_A = +25^{\circ}\text{C}$
3. See Bode plot on page 4.

TO-8 Metal Can



Package Dimensions

Heat Sinking

When operating the TP0032 at $T_A = +25^\circ\text{C}$, the case temperature will be approximately $+65^\circ\text{C}$. Although the TP0032 is specified for operation without a heat sink, bias current performance may be improved with the use of a small heat sink (Thermalloy 2241 or equivalent). The case has no internal electrical connection. It may be connected to the heat sink, although this will add capacitance to all pins and will probably necessitate compensation readjustment.

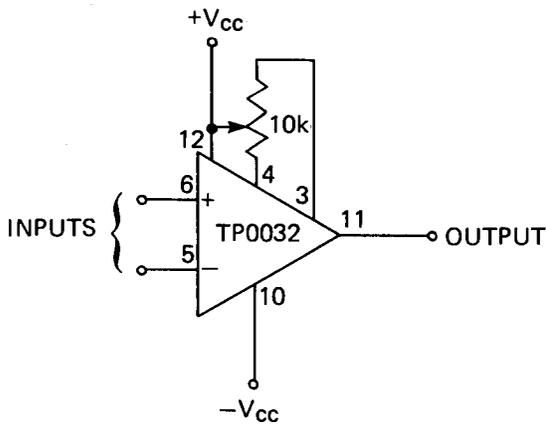
Wiring Recommendations

As with most high speed devices, the TP0032 is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible, with low inductance capacitors such as $0.01\mu\text{F}$ disc ceramics. Components for compensation should be located close to the appropriate pins to minimize stray capacitance. Good grounding techniques should be used.

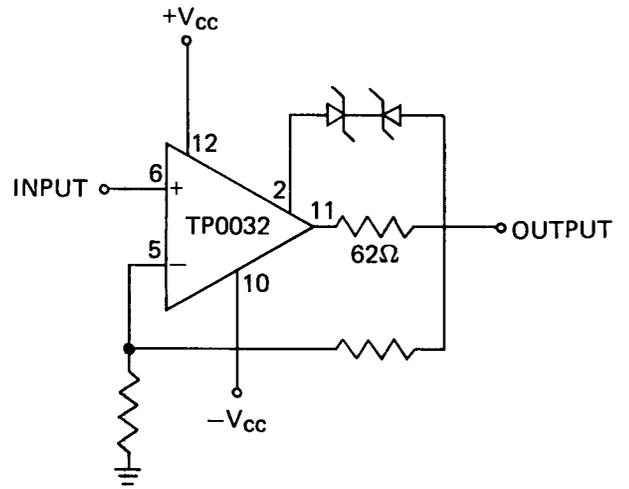
Input Capacitance

To compensate for the TP0032's 5pF input capacitance, it is recommended that a small capacitor be placed across the feedback resistor. The value of this capacitor will vary depending on the effects of layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

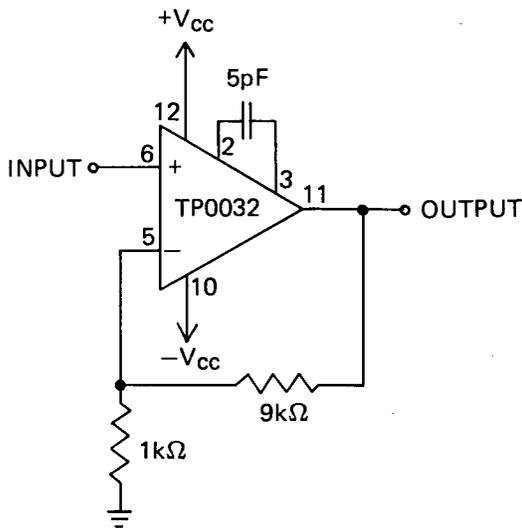
When using the TP0032 in a noninverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This practice will divert leakage currents away from the non-inverting input and reduce the effective input capacitance.



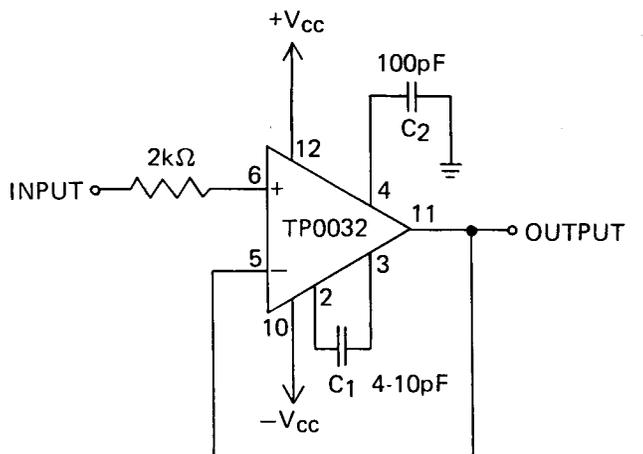
Offset Null



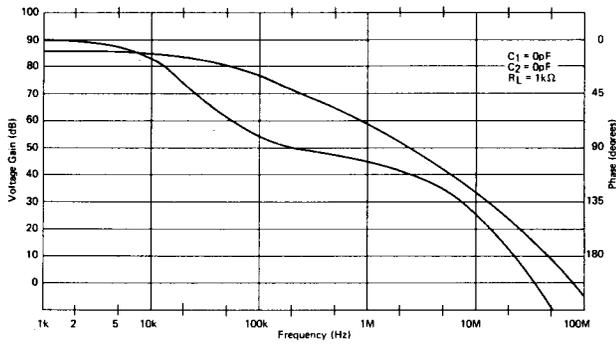
Output Short Circuit Protection



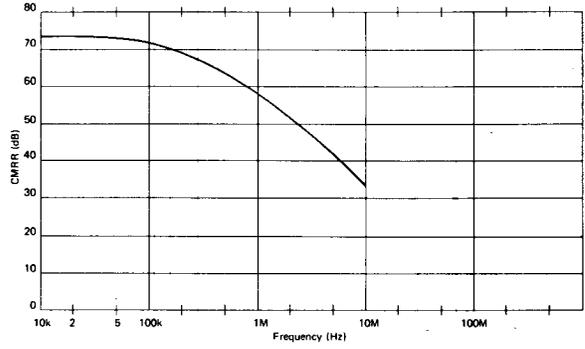
10 x Buffer Amplifier



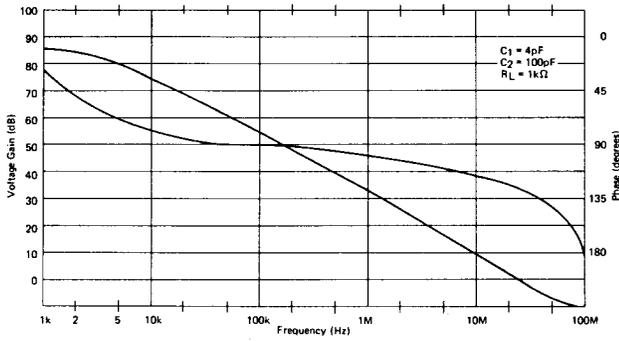
Unity Gain Amplifier



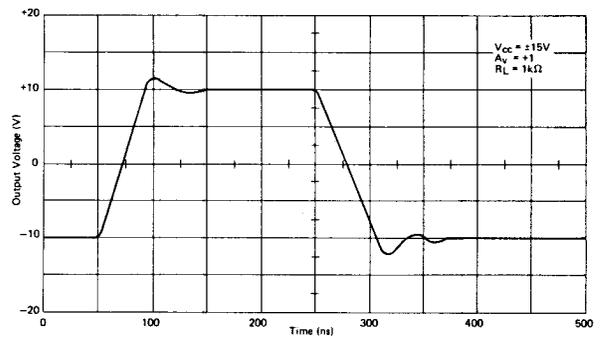
Bode Plot (Uncompensated)



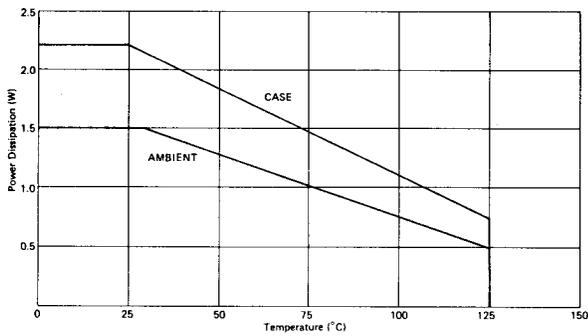
CMRR vs. Frequency



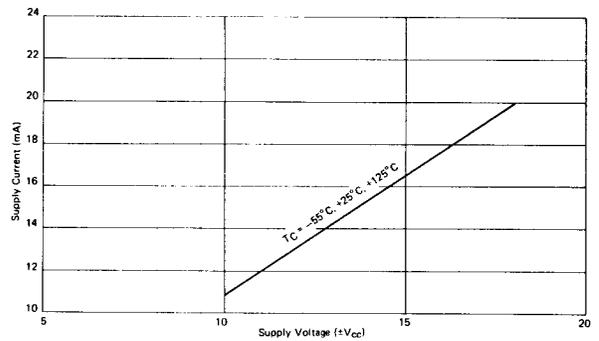
Bode Plot (Unity Gain Compensation)



Large Signal Pulse Response



Maximum Power Dissipation



Supply Current vs. Supply Voltage

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