Dynamic tests for op amps use synchronous demodulation

General-purpose technique is accurate, easy to use, gives direct meter readout and handles wide variety of tests

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Static tests for operational amplifiers are readily available in low-cost testers but dynamic tests—particularly for linear integrated-circuit op amps are more difficult, and suitable testers are hard to come by. The instrument must give accurate results for tests of open-loop gain, common-mode range and rejection, output swing, and power supply rejection. The user wants a unit that's easy to operate and, further, he'd like a direct readout. His requirements can be satisfied with an operational amplifier tester that uses low-frequency square waves and synchronous demodulation.

In the new synchronous detection method, the amplifier operates in a stable, closed-loop mode and thus is assured of operation in its linear region.

In most test methods, the output depends on the gain and when large signals are applied, there is a chance that the amplifier will be operating out of its linear region.

Three test methods

The advantages of the synchronous detection method are best demonstrated by first considering the drawbacks, of three other test schemes.

One is specified in the new military standard, MIL Std 883, as method 4004, section 1. In this method, an auxiliary amplifier is used to keep the amplifier under test zeroed for offset. To accomplish the zeroing the circuit, on top page 119, has two resistors, R_f and R_s. The source resistor, R_g, is made large in comparision with R_s to assure that only a small signal is applied to the circuit under test. Feedback capacitor, C_1, around the auxiliary amplifier, essentially opens the loop at the input signal frequency, which is typically in the range of 10 to 30 hertz. The output voltage and gain of the amplifier under test for this circuit are:

$$e_o = e_{in} \frac{R_s}{R_g + R_s} \cdot \frac{R_2}{R_1 + R_2} \cdot A_o$$

where

$$A_o = \frac{e_o}{e_{in}} \cdot \frac{1}{S}$$

$$S = \frac{R_s}{R_s + R_g} \cdot \frac{R_2}{R_1 + R_2}$$

If the input and output voltages of the amplifier under test are displayed as a Lissajous pattern the slope of the line, when properly scaled, represents the open-loop gain.

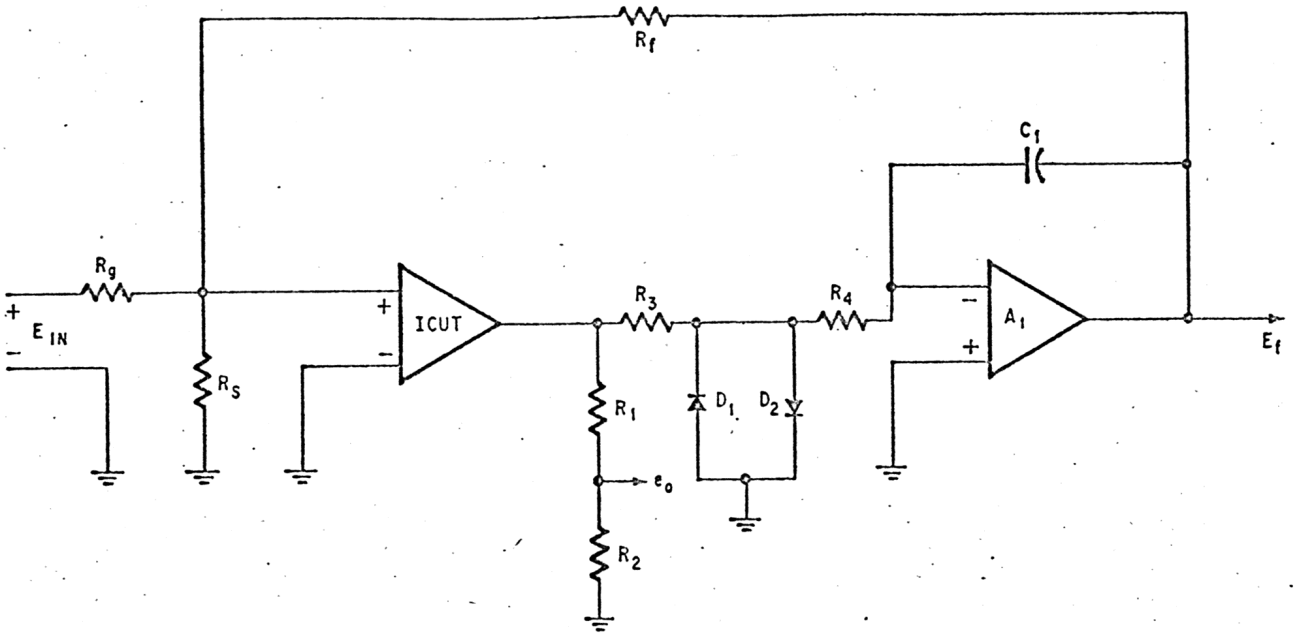
The two diodes clip the output of the amplifier so that no input offset voltage results because of an unsymmetrical output swing if the amplifier is overdriven. Such a condition can be observed on the oscilloscope and the linearity of the amplifier under test can be evaluated.

This method thus has the advantage of displaying gain, output swing and linearity simultaneously, with the additional benefit that all signals are high level, which eliminates any noise problems. However, it has some serious disadvantages.

First, the output level is directly dependent on the open-loop gain, which makes programing of output test conditions extremely difficult.

With the high gain, internally damped IC amplifiers now available, capacitor C_1 must have an extremely large value to open the loop adequately at the signal frequency.

The R_g-R_s attenuator must be very accurate and variable if IC amplifiers with wide variations in



Gain measurement. To determine the open-loop voltage gain for an integrated circuit op amp, A_1 must keep the IC under test (ICUT) zeroed for offset via resistors R_f and R_s. However, because C_1's value must be extremely large, the circuit is impractical.

parameters are to be tested. Hand programing is mandatory.

Finally, the readout device—the oscilloscope—is not easily adaptable to a direct reading meter.

The second method, below left, is far simpler than the first but has all its drawbacks. It consists of a simple feedback circuit with an attenuated input applied to the amplifier under test. For an a-c signal, the gain will be

$$A_o = \frac{R_g + R_s}{R_s} \cdot \frac{e_o}{e_{in}}$$

This circuit does not allow the amplifier under test to be overdriven as the square wave output tends to rebias the IC, changing its response.

The third method, given in the new military standard, is also simple, see below right. The signal is applied to the amplifier under test through a voltage divider, coupling capacitor, and feedback resistor, R_1, with a shunted resistor from one terminal of the amplifier to ground. Under the condition that

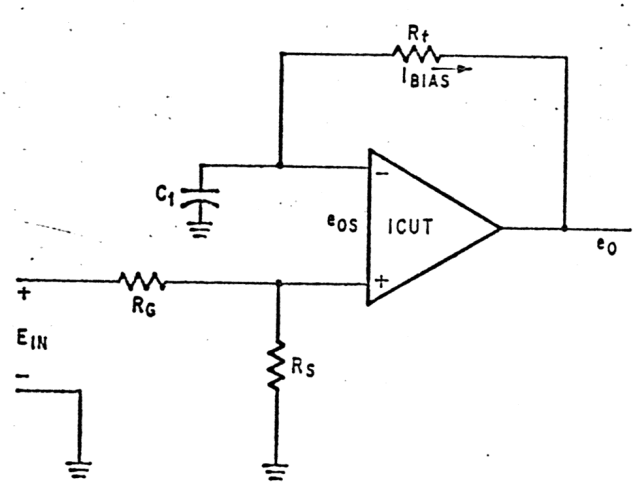
$$\frac{(A_o + 1)\,(R_3 \| R_4 - j\,X_{c1})}{R_1} < 0.1$$

the open-loop gain is

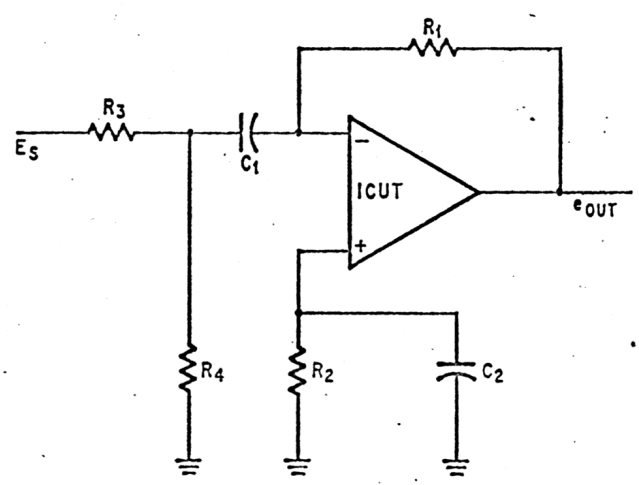
$$A_o = \frac{e_o}{e_s} \cdot \frac{R_3 + R_4}{R_4}$$

$$R_3 \gg R_4$$

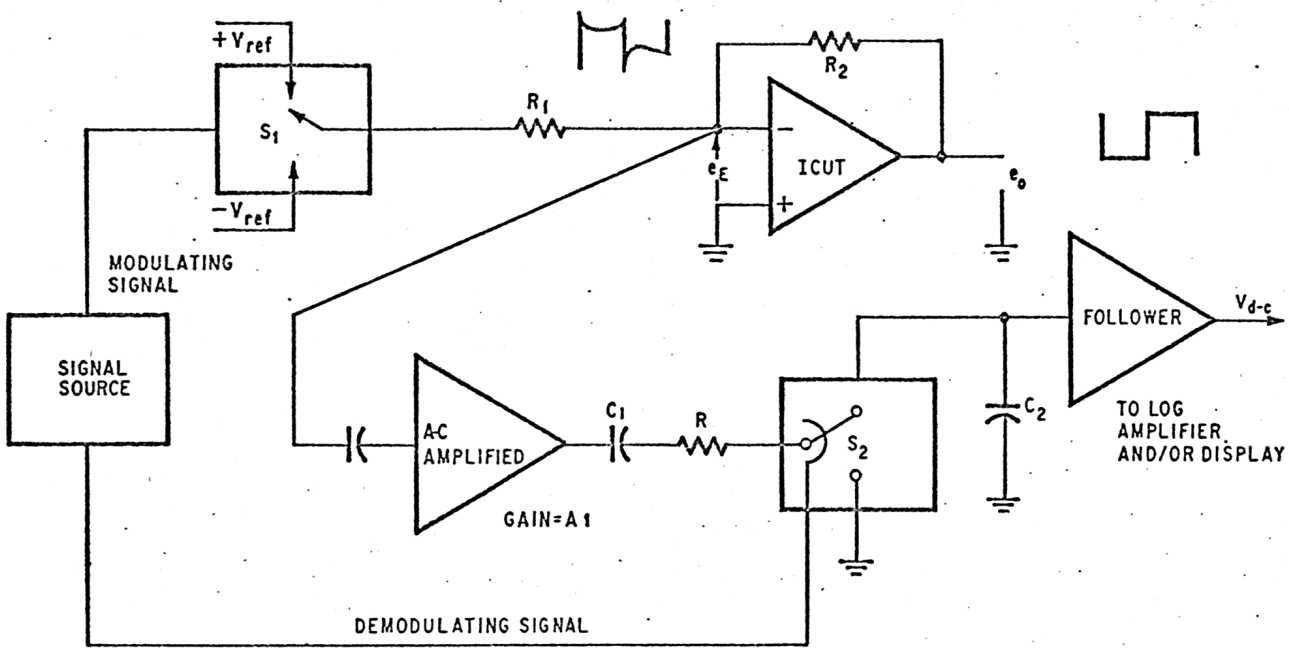
The imposed condition requires that the closed-



Voltage gain. Output e_o at d-c is equal to the input offset voltage plus the drop across the feedback resistor, $I_{bias}R_f$. Circuit cannot be overdriven because the output tends to rebias the IC, thus changing its open-loop response.



Voltage divider method. Closed-loop gain must approximate the open-loop gain by 90% for this test setup to be effective. However, this means that the circuit will be unstable, and therefore, is not a practical measurement scheme.



Synchronous detections system. Error voltage, e_E, developed at input of integrated circuit under test is amplified and demodulated by switching circuit S_2. Both S_1 and S_2 are synchronized, causing C_1 to charge to V_{ref}.

loop gain approaches the open-loop gain within 90%. Thus the stabilizing effect of the feedback has been lost, making the output signal gain depend on the gain again.

The method is thus an impractical way of characterizing the open-loop response of an amplifier. For example, suppose that the amplifier has an open-loop gain, A_{vo} of 100,000 volts,/volt, a unity gain-bandwidth product, f_t, of 1 megahertz, and a feedback resistor, R_1 of 10 kilohms. For conditional equation to hold,

$$R_3 \parallel R_4 - j\,X_{c1} \leq 0.01$$

Suppose R_3 is much greater than R_4 so that the parallel combination is approximately equal to R_4

and that $X_{c1} \leq 0.1\,R_4$

then $R_4 \leq 0.01$ ohm

and $X_{c1} \leq 0.001$ ohm

With a 6 decibels/octave roll-off, the first open-loop break occurs at a frequency of 10 hertz. Thus to get an accurate determination of the gain, the measurement must be performed at or below this frequency. At 10 hertz, the value of C_1 must be

$$C_1 = \frac{1}{2\pi \cdot 10 \cdot 0.001} = 16 \text{ farads}$$

which is hard to come by.

Synchronous detection

In the synchronous detection method, the input to the test circuits is a square wave produced by switching between two stable d-c references. This allows a-c coupling in the system. The voltage signal from the unit under test is amplified further with precision, and then band-limited to reject d-c drift, very low frequency noise (flicker), and high frequency noises.

The amplified signal is demodulated or converted back to a d-c signal with a peak-to-peak detector switching in synchronism with the input signal. Because synchronous demodulators inherently provide improved signal-to-noise ratios, low level signals on the order of microvolts can easily be detected.

The operation of a synchronous detection system is detailed above. The magnitude of the d-c reference voltages should be at least as great as the largest voltage encountered when testing the unit for the amplifier to operate with a small closed-loop gain or in a common-mode configuration, requiring a large signal to swing the amplifier over its full range.

The output of the amplifier under test is

$$e_{o,p\text{-}p} = \frac{R_2}{R_1} \cdot 2|V_{ref}|$$

As the amplifier is running in a closed-loop mode, a gain-error signal (e_E)

$$e_E = -e_o/A_o$$

appears between the negative input terminal and common, where A_o is the open-loop gain of the amplifier under test.

This error is a-c coupled, and amplified to an appropriate level before being demodulated by switching circuit S_2, since the signal source drives S_2 in synchronism with S_1. Capacitor C_1 charges to V_{ref} in a negative direction with respect to ground on one half cycle. On the next half cycle, C_2 charges in a positive direction.

After a few cycles, a d-c signal appears across C_2 equal to the peak-to-peak value of the gain error signal multiplied by the appropriate a-c gain. This d-c signal is

$$V_{d\text{-}c} = e_E \cdot A_1$$

Where A_1=gain of the a-c amplifier.

Thus

$$A_o = A_1 \cdot \frac{R_2}{R_1} \cdot \frac{2|V_{ref}|}{V_{d\text{-}c}}$$

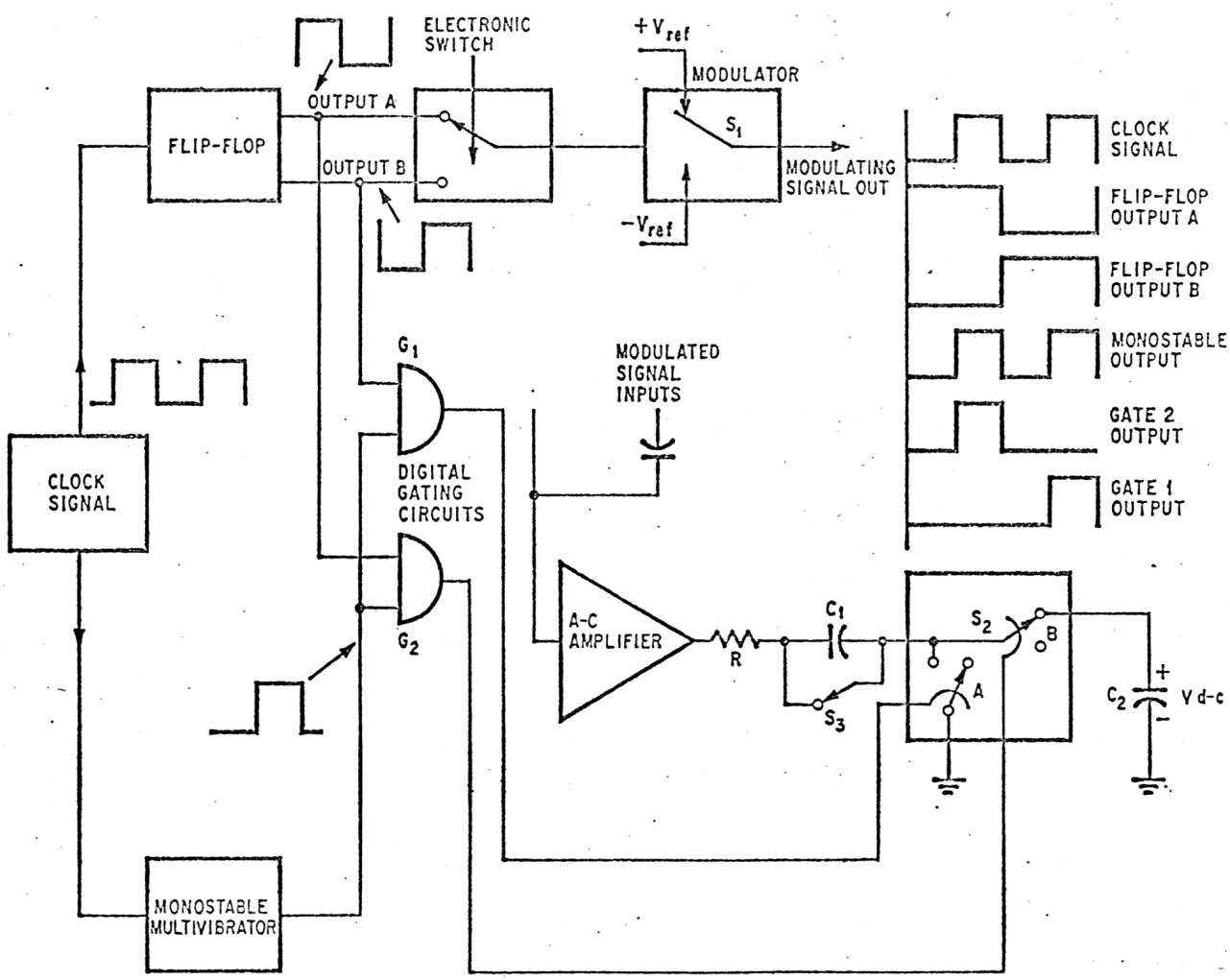
This d-c signal could be used to drive a logarithmic amplifier for direct readout in decibels with a DVM, go-no-go discriminator, or analog-to-digital converter, however, this basic circuit requires some precautions.

The switching signal must be of low enough frequency that the transient spikes on the detected signal introduce minimal error. The maximum repetition rate will be determined by the low-frequency open-loop characteristics of the amplifier under test. Some form of protection is needed for the input terminals of the amplifier under test.

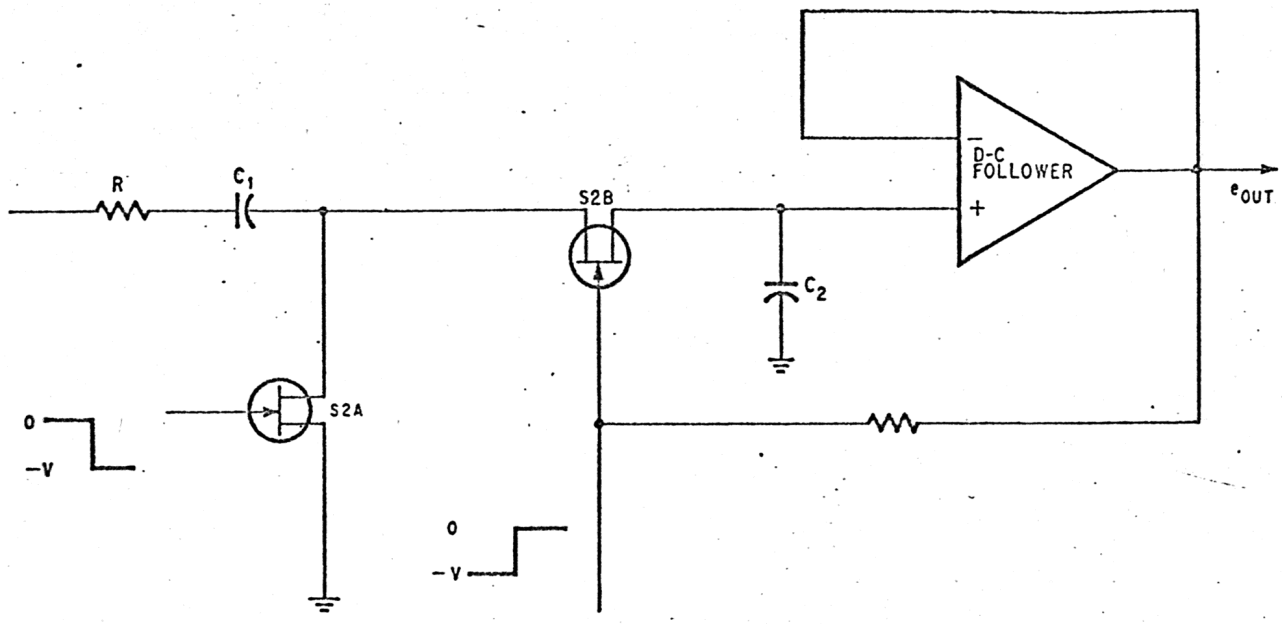
The a-c amplifier must be able to pass the low frequency square waves encountered and its output impedance must be relatively low to allow C_1 and C_2 to charge quickly. Finally, the d-c follower must have a very high impedance input (preferably a field-effect transistor type) so not to discharge C_2 on alternate half cycles.

The system can be improved and some of the above problems overcome by modifying the circuit to include a clock signal and sequential logic as shown below. The input signal operates a flip-flop whose output drives an electronic switch. The electronic switch output drives the modulator which in turn feeds the square-wave signal to the test circuit. The electronic switch allows the modulating signal to be put into or out of phase with the original switching signal in order that the output may be of the desired polarity. The clock signal also drives a monostable whose output is gated with the flip-flop outputs.

The flip-flop causes the modulating frequency to be one-half the clock frequency. The flip-flop is designed to trigger on the negative slope and the monostable on the positive slope of the clock output. This causes gates G_1 and G_2 to function only on the latter half of each switching period, by which time, nearly all transients on the error signal (to be demodulated) have damped out.



Modified synchronous system. Adding a clock signal and sequential logic to the basic synchronous system eliminates the need for a low output impedance for the a-c amplifier and a high input impedance for the d-c follower.



Synchronous demodulation. Because of its wide dynamic range, this demodulator is used to drive a logarithmic amplifier and display. Charging period of each capacitor is controlled independently of the detected signal, and sampling occurs only when a signal is present.

When gate G_1 is turned on, C_1 is grounded by S_{2A}. At the same instant, G_2 is off, opening switch S_{2B}.

We now have a synchronous sample-and-hold peak-to-peak detector, where the sampling period is set by the timing cycle of the monostable multivibrator.

To allow direct measurement of d-c levels, as well as peak-to-peak amplitudes, one may direct couple the a-c amplifier and short-circuit capacitor C_1 with S_3. Now the system is a synchronous peak reader. By changing the phase of the modulating signal with the electronic switch, signals of either polarity from the amplifier under test can be measured under dynamic conditions. This feature allows the measurement of maximum output under load as well as common-mode range.

Demodulation

The demodulator circuit consists of two junction field-effect transistors operated in a shunt-series chopper configuration, is shown above. The gate signal for the shunt FET is referenced to ground; the gate signal for the series FET is referenced to the d-c follower output. This assures that the FET's will be either on or off. Using a good FET input operational amplifier for the follower, signals ranging in level from a few millivolts to 10 volts are accurately demodulated. The only significant error of this circuit is that produced by the follower's offset and drift. This circuit has a wide dynamic range that is used to advantage to drive a logarithmic amplifier and display.

The circuit has several advantages over a conventional diode voltage doubler. The charging period of each capacitor can be controlled independently of the magnitude of the signal being detected. This permits sampling only when a signal is known to be present—the circuit ignores transients. Second, the reaction or settling time at slow sampling rates is much faster than with diodes for several reasons:—charging is better controlled because small capacitors can be used due to low FET leakage during the hold interval; and discharging is better controlled because the path is through the relatively low impedance of a turned-on FET, and not through the exponentially varying impedance of a diode. Third, a large dynamic range is possible. This is in contrast to a conventional doubler circuit where diode leakage during the hold period causes ripple, which introduces significant errors, especially at low signal levels.

To measure open-loop gain, the ratio of the change in output voltage to the change in input, a more suitable test circuit is the one at the top left of page 123. The output voltage is

$$e_{out} = -\frac{R_f}{R_g + R_s} \cdot \frac{1}{1 + \frac{1}{A_o B}} \cdot V_{ref}$$

where

$$B = \frac{1}{\left(1 + \frac{R_1}{R_2}\right)\left(1 + \frac{R_f}{R_f + R_g} + \frac{R_f}{R_1 + R_2}\right)}$$

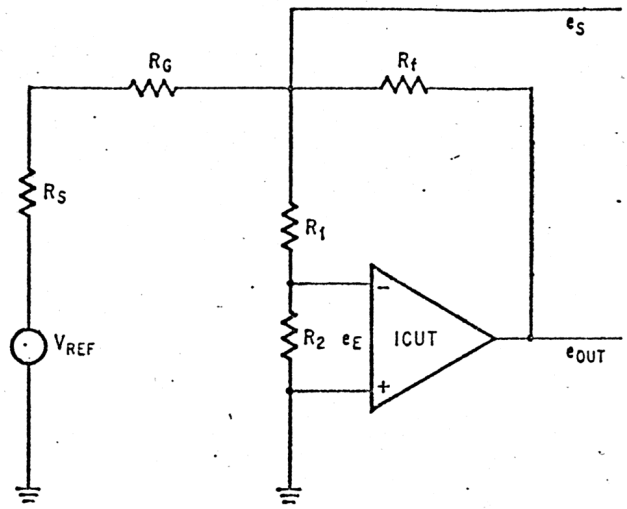
and

$$e_s = -\left(1 + \frac{R_1}{R_2}\right) \cdot \frac{e_{out}}{A_o}$$

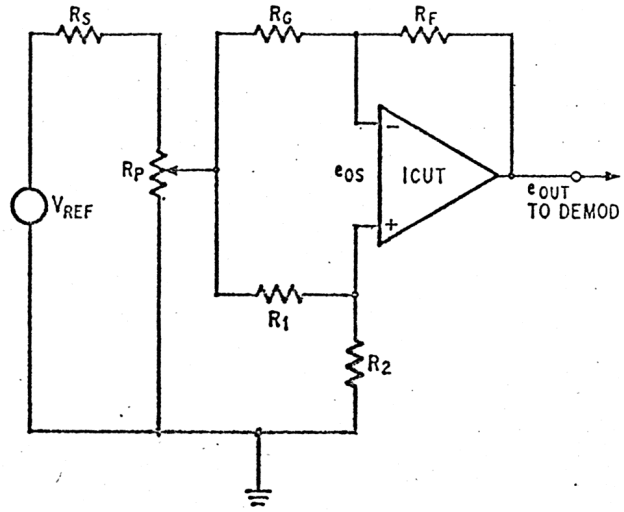
A_o=open-loop gain= $\Delta e_{out}/\Delta e_E$

R_s=source impedance of synchronous modulator

By a careful choice of values, one can make $1/A_oB$ small, less than 0.01, resulting in less than 1% error for the following approximation:



Gain circuit. Because the output signal, e_{out}, is predictably set and measured by the synchronous demodulator, the gain is easily computed logarithmically and can be displayed on a read-out device.



CMRR tester. Common-mode rejection ratio, CMRR is dependent on the input common-mode voltage and the change in offset voltage that results from a common-mode swing.

$$e_{out\ p\text{-}p} = 2|V_{ref}|\frac{R_f}{R_s + R_g}$$

Keeping this in mind, one can easily program the output level of the amplifier under test with a single precisely-calibrated resistor (R_g) on a program card. This will allow the same basic circuit to measure gain of different devices having different swing capabilities.

The gain equation is:

$$A_o = \frac{e_{out\ p\text{-}p}}{e_{s\ p\text{-}p}}\left(1 + \frac{R_1}{R_2}\right)$$

Because e_{out} is predictably set and e_s is measured by the synchronous demodulator, the gain can be easily computed logarithmically and displayed in db on a read-out device. The purpose of voltage divider R_1 and R_2 is to increase the measured error signal and eliminate the need for additional a-c gain. Also, by attenuating any applied inputs, it limits the signal that can appear differentially across the IC's inputs, thus affording a degree of protection. These resistor values are restricted somewhat by the maximum bias and offset voltage of the device under test as well as the gain-error criteria stated in the gain-error equation.

Common-mode rejections ratio (CMRR) is defined as the ratio of the peak-to-peak input common-mode voltage to the peak-to-peak change in input offset voltage that it produces. The test circuit is at the above right. In the circuit,

$$e_{cm} = \frac{R_2}{R_1 + R_2}\, e_{in}$$

The common-mode input offset voltage, (eos) resulting from a common-mode swing is now defined as that voltage needed between input terminals to drive the amplifier output to zero when the inputs are swinging together.

The common-mode rejection is

$$\text{CMRR} = \frac{e_{cm}}{\Delta e_{os}} = \frac{e_{in}}{e_{out}} \cdot \frac{R_f}{R_g}$$

where e_{cm} is the actual common-mode voltage, and e_{in} is the driving function. This last expression for CMRR is valid provided the following condition is satisfied:

$$\frac{R_2}{R_1} = \frac{R_f}{R_g}$$

For imbalances in the resistor ratio, the actual expression for e_{out} vs E_{in} becomes

$$\frac{e_{out}}{e_{in}} = \frac{R_f}{R_g}\left[\frac{1+\frac{R_g}{R_f}}{1+\frac{R_1}{R_2}} \cdot \frac{1}{\text{CMRR}} + \frac{\frac{R_g}{R_f} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}}\right]$$

From this equation, one is able to determine how closely the resistor ratios must be matched for the first equation to be valid with any given CMRR and allowable error. Ways to achieve the required balance are to use precision resistors and to make R_2 adjustable by inserting a variable resistor in series.

The voltage divider R_p allows programing the common-mode voltage desired. The driving signal again comes from the synchronous modulator, and the output of the test circuit is detected by the synchronous demodulator circuit.

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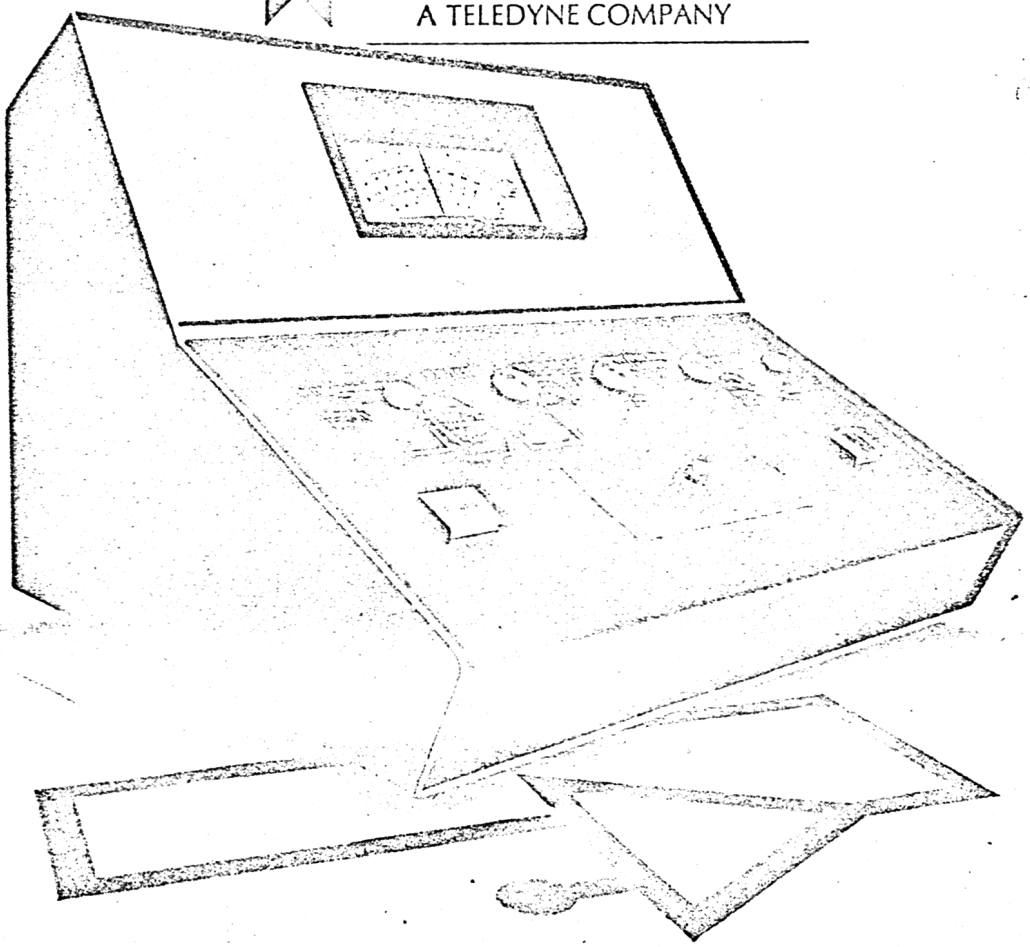

Circle 189 on reader service card