TELEDYNE PHILBRICK

4705/4707/4709

1 MHz / 5 MHz / 100 kHz LOW DRIFT VOLTAGE-TO-FREQUENCY CONVERTERS

The 4705, 4707, 4709 Family of High Performance Voltage to Frequency Converters provide precision conversion of analog voltage - data - to a train of pulses whose repetition rate or frequency is a direct linear function of that analog voltage over a nominal range of 0 to +10 V. These versatile devices perform a wide range of data acquisition, transmission, and recording functions and, in addition, are capable of unique signal processing activities which include frequency multiplication, digital to frequency conversion and infinite hold time integration.

Note: Throughout this data sheet, Full Scale is denoted by FS.

BASIC CONNECTIONS & TRIM

Positive Input Signals

These Voltage to Frequency Converters are factory trimmed to a zero and full scale accuracy of better than 1 part in 1000. Thus for most positive voltage input applications they are connected as shown in Figure 1 without the addition of trim components. This produces a TTL compatible output pulse with nominal width equal to 1/3 the period of device Full Scale Frequency.

Zero & Full Scale Trim (Input to $+V_{in}$ Pin)

When greater accuracy is required, input offset voltage (E_{OS}) and Full Scale (FS) output frequency are trimmed with external potentiometers as shown in Figure 2.

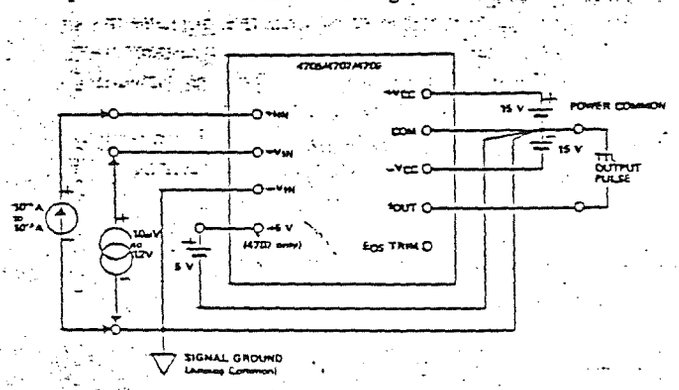
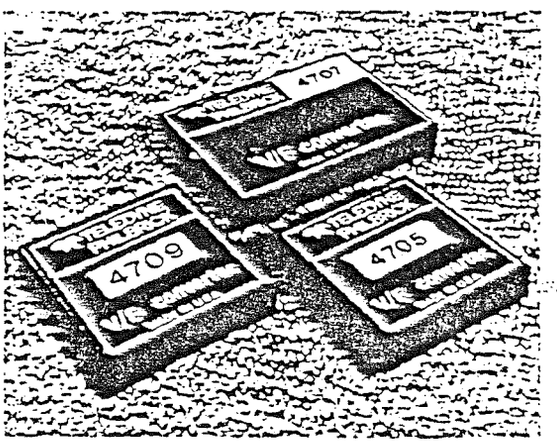


Figure 1. Positive Input Signals



FEATURES

- ±12 ppm/°C Max. Stability
- Wide Operating Range, 0.1 Hz to 5 MHz
- Resolution equivalent to more than 16 Bits
- High Noise Rejection
- Current-to-Frequency capability
- 0.005% Nonlinearity
- Dynamic Range equivalent to 20 Bits
- Low Cost

APPLICATIONS

- Process Transducers
- Voltage or Current Sources
- High Resolution, Video/Optical Data Link
- Digital Frequency Synthesis
- Wide Range Phase-Locked Loops
- No Drift Integrate/Hold
- High-Voltage Isolation
- DVM's or DPM's
- 2-Wire Digital Transmission
- Telemetry
- Analog to Digital Converters
- Servo Loops
- Synchronous Speed Control

SPECIFICATION SUMMARY

		4705	4705-01	4707	4709	4709-02
Full Scale Frequency FS f_{out} for +10 V in		1 MHz	1 MHz	5 MHz	100 kHz	100 kHz
Max Nonlinearity ±% FS ±% Signal		0.001 + 0.05	0.0005 + 0.02	0.01 + 0.05	0.005 + 0.02	0.005 + 0.02
Max Full Scale TC ± PPM/°C		200	200	100	44	12
f_{out} Max/f_{out} Min = Dynamic Range Decades		6	6	5	6	6
INITIAL ACCURACY (Untrimmed)	ZERO	10 mV Max (trimmable to zero)			3 mV Max (trimmable to zero)	
	FULL SCALE	+9.900 ± 0.05 V in for Full Scale Frequency Out (trimmable to +10 V)				

1. Apply 10 mV between R1 and Signal Ground. Adjust R2 for f_{out} = Full Scale Frequency divided by 1000.
2. Apply 10 V between R1 and Signal Ground. Adjust R1 for f_{out} equals device Full Scale Frequency.
3. Repeat (1) and (2) for precise Zero & Full Scale set.

Note: All fixed and variable trim components should have temperature coefficients similar to that of the V to F being used, e.g., they should be wire wound, metal film or cermet.

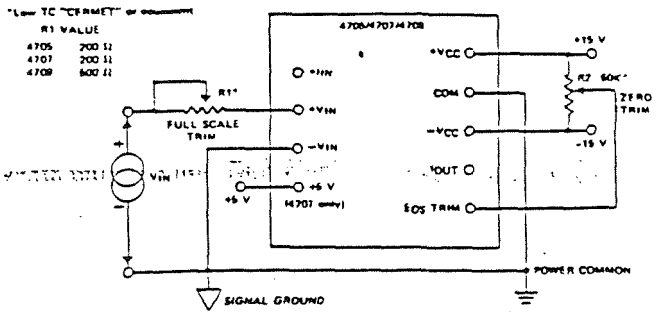


Figure 2. Zero & Full Scale Trim
Positive Voltage Input

Negative Input Signals (Input to $-V_{in}$ Pin)

The 4705 and 4707 can operate with negative input voltages as great as 1 V applied to the $-V_{in}$ pin as shown in Figure 4B. This one volt signal will produce a Full Scale Output Frequency of 1/10 the specified Full Scale Frequency. The 4709 can be operated with up to −50 mV at the $-V_{in}$ pin. To obtain specified Full Scale output frequency for an input voltage of less than plus or minus 10 volts, see Full Scale Factor Change. It should be noted that input impedance at the $-V_{in}$ pin is typically greater than 10 Meg ohm.

Zero & Full Scale Trim (Input to $-V_{in}$ Pin)

Zero Trim is performed with R2 as shown in Figure 2. For Full Scale Trim, connect R1 between $+V_{in}$ and Signal Ground.

Follow the Trim Procedure for signals at the $+V_{in}$ pin.

Current Input (Signal to $+I_{in}$ Pin)

The Full Scale Current Sensitivity I_{FS} of each V to F model has a tolerance of about ±25%. The exact I_{FS} may be set using the circuit of Figure 5A.

THEORY OF OPERATION

To take maximum advantage of V to F versatility, a functional block diagram (Figure 3) and theory of operation is provided. With this information, input and output circuitry are easily modified to handle virtually any signal or load.

The V to F is a free running (astable) voltage controlled multivibrator (see Figure 3). The effective currents from the four inputs (A, B, C, and D) are summed at the minus input of op amp A1. A1 and transistor Q1 form a precision current pump, producing current I from the collector of Q1, which is a linear function of the A1 input currents. Current I charges capacitor C at a rate which is a precise linear function of the V to F input.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt-Trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a constant width output pulse. This pulse performs two functions. Amplified by Q2, it is the output of the V to F and it functionally activates the Precision Charge Dispenser (PCD). The PCD discharges C to the same reference level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the input signal, producing the waveforms shown in the timing diagram, Figure 7. That is, the rate of charging C, (the repetition rate of charging C and thus the output frequency) are functions of the V to F voltage and/or current inputs.

TRIM THEORY

The V to F input circuit Zero and Full Scale trim techniques are based on the input circuit amp (A1, Figure 3) and the user may treat the input as such within certain limits. No combination of signals may be applied to the inputs which will drive the A1 output positive. That is, a frequency output will not result if the total current into the positive inputs (A1, summing point) becomes negative with respect to the negative input. If this occurs, D1 will become forward biased, Q1 cut off, I becomes zero, and f_{out} becomes zero. The inherent current Full Scale Factor has a tolerance of ±25% to give specified Full Scale frequency out. Resistor R1 factory trims the full scale $\pm V_{in}$ to within ±0.5%.

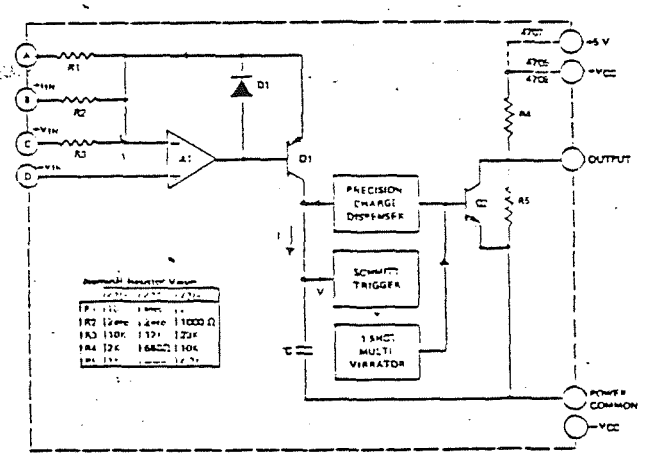


Figure 3. V to F Simplified Block Diagram

FULL SCALE FACTOR CHANGE

The Specified V to F Full Scale Factor is 9.9 V ±0.05V to produce Full Scale Frequency out. Many applications require FS f_{out} for other (larger or smaller) Full Scale input signals and polarities. Figures 4A through 4F illustrate how to operate these V to F's with such signal levels.

Magnitude of V_{in} > 10 Volts

The 4705, 4707, and 4709 can be operated with input voltages greater than +10 V by connecting a fixed resistor and trim potentiometer in series with the + voltage input (see Figure 4A). For voltages more negative than −10 V, the attenuator network of Figure 5B performs well. Zero Trim and other adjustments remain the same as for Figure 2.

If the full scale input voltage is between +0.1 V and +10 V, the full scale output is set by using the + current input terminal with a series resistor as shown in Figure 4C. The only effect will be to reduce dynamic range since the minimum input voltage does not change from 10 μV. To keep a 120 dB dynamic range, use Figure 4D.

When the Full Scale Input Signal is between −0.1 volts and +0.1 volts, a low drift amplifier such as the TP 1703 should be used to raise the signal to 10 V. See Figure 4D.

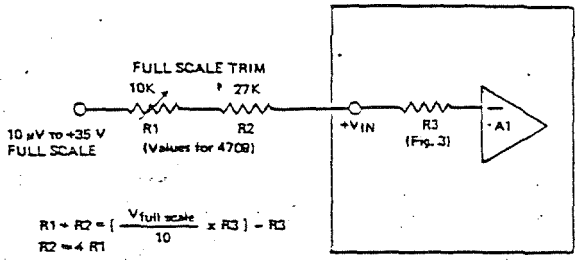


Figure 4A. Full Scale +V_{IN} Greater than +10 V

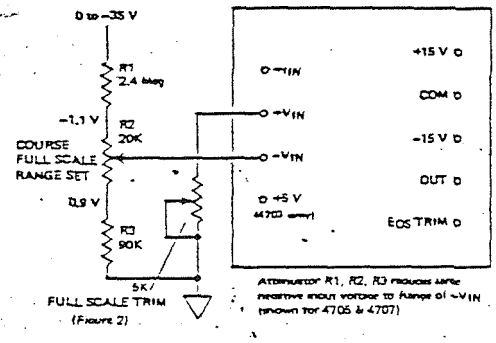


Figure 4B. Full Scale Input Voltage More Negative than −10 V

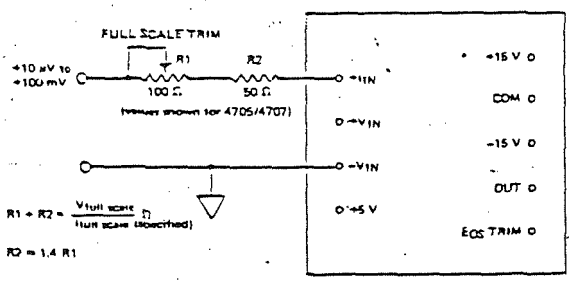
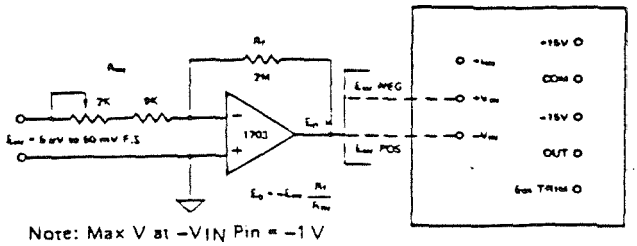


Figure 4C. Full Scale Input Between ≈ +0.1 V and +9.9 V



Note: Max V at −VIN Pin = −1 V

Figure 4D. Full Scale Input Voltage Between −.1 V and + .1 V

Reduce Full Scale f_{out} Below Specified FS f_{out}

In some applications, a Full Scale output frequency of less than specified Full Scale is required when the input signal is 10 volts or greater. The circuits of Figures 4 and 5 which show attenuation of the input signal to 10 volts are used to decrease the Full Scale input signal below 10 V and, therefore, decrease Full Scale f_{out}.

To maximize use of the dynamic range, the input signal is conditioned to +10 V or −1 V and a binary or BCD frequency divider (counter) is connected to the output. Any TTL, CMOS, or HNIL device may be used, from a simple divide by 10 unit to the CMOS DC4059, which can divide by any number from 3 to 15,999.

If, for example, the 4709 FS output is set at 100 kHz, as shown in Figure 4E, counter output will be 10 kHz while the minimum output frequency will be 10 mHz.

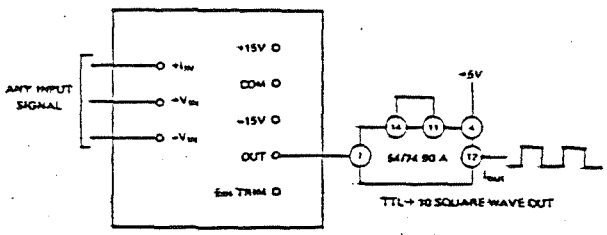


Figure 4E. Full Scale Output Less Than Specified When VIN is Equal To Or Greater Than 10 V

Full Scale Input Current Greater Than Specified

If the full scale input current is greater than +200 μA, the "current splitter" circuit of Figure 5A is used. As noted in Figure 5A, the voltage developed at the wiper of the potentiometer must be less than the compliance voltage of the current source. A negative input current is conditioned by passing it through a resistor connected between $-V_{in}$ and signal common and thus producing a negative voltage. (Trim with pot between $+V_{in}$ and common.) The compliance voltage of the current source must be greater than the maximum voltage developed across the resistor.

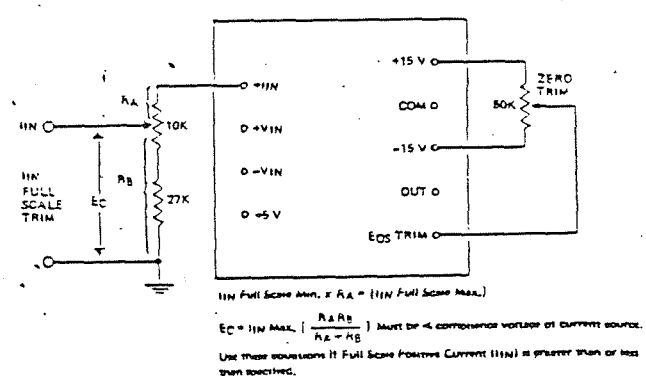


Figure 5A. Zero & Full Scale Trim for Positive Input Currents

The best way to CONDITION CURRENT SIGNALS is with the classic current to voltage converter circuit shown in Figure 5B. With this circuit and the "right" amplifier, virtually any current (even femtoamps) will provide a positive or negative full scale input with no compliance voltage problem.

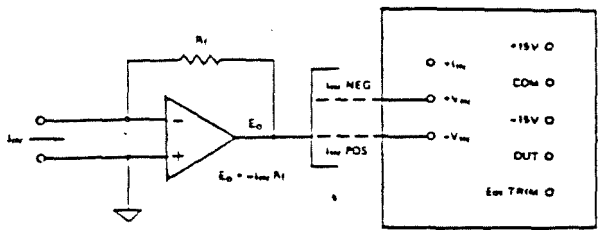


Figure 5B. Full Scale Input Currents Negative Of Less Than 200 μA

OPERATION WITH BIPOLAR, FAST, or NON-ZERO BASED INPUT SIGNALS — "OFFSETTING"

Many V to F applications require operation with bipolar input signals (e.g. −5 V to +5 V). In other applications the input signal is changing rapidly (e.g. ±1V @ 10 kHz). In still others the input signal does not pass through zero (e.g. +6 V to +8 V).

Such signals cannot be handled by V to F's when connected as illustrated in Figures1'through 5. However, their versatile op amp input circuit is easily adaptable to these signals through the technique of OFFSETTING. It is implemented by the application of a fixed OFFSET signal to one of the three V to F inputs, usually such as to produce an output or OFFSET frequency when the input signal of interest is zero. Essentially, the OFFSET voltage or current is algebraically added to the signal of interest at the op amp summing point. The effective input resistor for the plus and minus V_{in} pins is R3 in Figure 3. A different OFFSET technique is required for each of these three types of input signals, therefore, they are described separately.

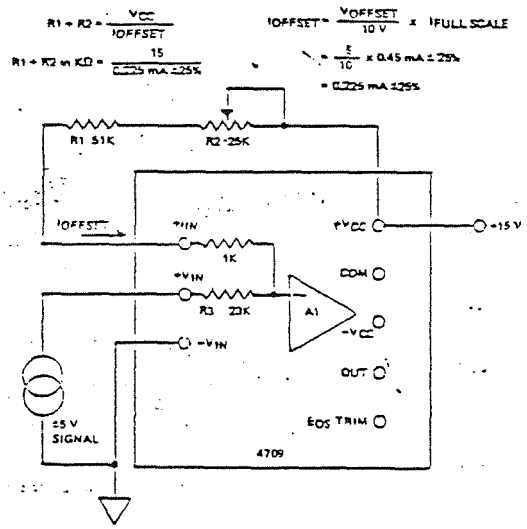


Figure 6A. V to F With +5 V Offset
Allows Operation With Bipolar ±5 V Input Signal

Operation With Bipolar Input Signals

A ±5 V signal connected to the $+V_{in}$ pin of a 4709 as shown in Figure 2 will produce no output from −5 V to 0 V and 0 to 50 kHz out from 0 V to +5 V_{in}. Essentially an OFFSET of +5 V (½ Full Scale) must be added to the +5 V input voltage to produce 0.1 Hz out for +5 V_{in}, 50 kHz out for 0 V in and 100 kHz out for +5 V_{in}. This may be accomplished as shown in Figure 6A by injecting an offset current into the $+I_{in}$ pin through R1 and R2. This is the equivalent of connecting a resistor, with the same value as the $+V_{in}$ input resistor (23K), to +5 V.

Operation With Non-Zero Based Signals (Figure 6B)

When the signal of interest is a small changing voltage impressed on a fixed DC voltage, the $+V_{in}$ pin is offset to eliminate the fixed voltage while the signal is applied to the $+I_{in}$ pin to provide a scale factor increase. For example, in Figure 6B a 2 V signal is impressed on a fixed +15 V. The +15 V is offset to zero by summing it through R1 and R2 at the op amp $+I_{in}$ pin with −15 V from $-V_{cc}$ through the 10K $+V_{in}$ input resistor. R1 and R2 reduce the scale factor so the 2 volt signal provides a full 1 MHz out from the 4705. The 50K offset trim pot is used to set the minimum f_{out}, while R1 sets maximum f_{out}.

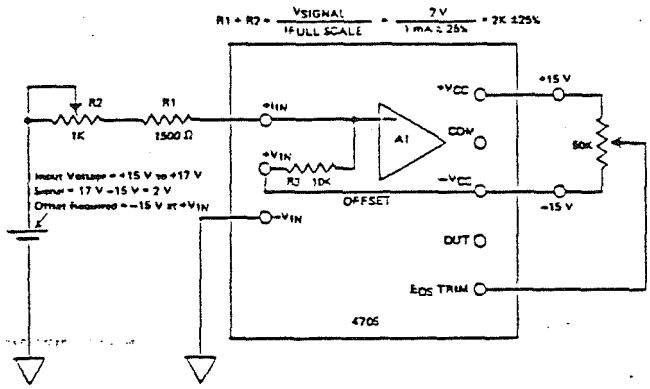


Figure 6B. V to F with −15 V Offset
Allows Operation with Small (2 V) Signal
Impressed on Larger DC Voltage (+15 V)

Operation With Fast Signals (FM Modulation)

A basic V to F application requires operation with DC to high frequency input signals (for example, a fiber optic FM data link with response from DC to 50 kHz). To accurately handle this signal the output of the V to F must be able to change much faster than the input. The basic response time of a V to F is one period of the new frequency plus approximately 5 μsec. For example, if the input of a 4707, 5 MHz V to F is changed one volt from 1.01 volts to 0.01 volts the new frequency is 5 kHz and response time is 1/5 kHz +5 μsec or ≈205 μsec. When the input changes from 11 volts to 10 volts the new frequency is 5 MHz and response time is ≈5.2 μsec. If the system is to accurately follow a 50 kHz input sine wave, V to F response must be less than 1/10 the period of the signal of interest. This is accomplished as shown in Figure 6C by offsetting the V to F output to 2.5 MHz with +5 V at the $+V_{in}$ pin and connecting the ±1 V signal to the $-V_{in}$ pin.

Operation With Differential Input Signals (4705, 4707)

The $+V_{in}$ and $-V_{in}$ pins of the 4705 and 4707 represent a differential input capable of accepting a ±1 V signal from a balanced line or bridge transducer and rejecting any common mode voltage. This ability often eliminates the need for a differential amplifier. However, to effectively use this pair of input terminals differentially, several simple conventions (definitions) must be observed as illustrated in Figure 6D.

1. Common Mode Voltage (CMV) is defined as the voltage between $\pm V_{cc}$ common and the negative V_{in} pin.
2. The positive V_{in} pin must always be positive with respect to the negative V_{in} pin.
3. CMV Range is typically ±1 V.
4. The differential (floating, balanced) signal source must be returned to $\pm V_{cc}$ common through a resistance and must not create voltages which exceed the limits set by 1, 2, and 3.
5. $f_{out} = \dfrac{(+V_{in})-(-V_{in}) \times FS\ f_{out}}{10\ V}$

Note: The 4709 may be operated in a similar manner but the maximum CMV is ±100 mV.

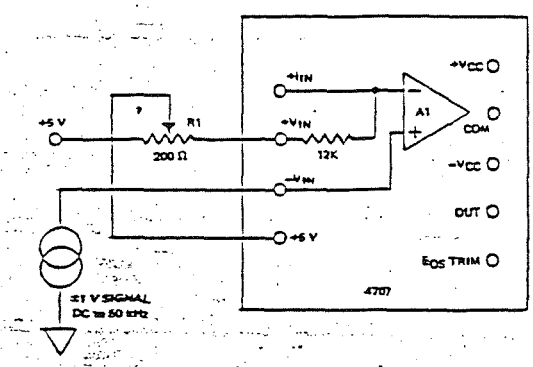


Figure 6C. V to F With Offset (+5 V) To Provide Fast Response (50 kHz)

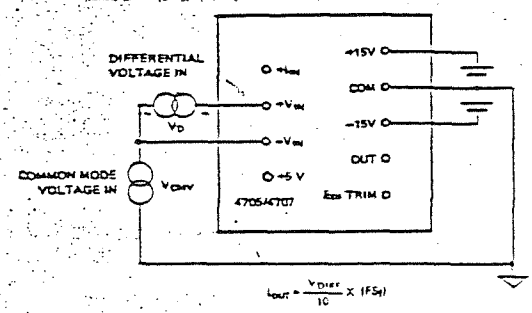


Figure 6D. Definition of Differential & Common Mode Voltage

OUTPUT CIRCUIT

Wave Form

The output circuit of each V to F (see Figure 3) is designed to drive 10 TTL loads. However, each is slightly different to maximize the speed power trade off. Output pulse amplitude of the 4705 and 4709 may be increased by shunting R4, or decreased by shunting R5. This will also increase rise time and the ability to drive a capacitive load.

Figure 7 illustrates typical output pulse shape, timing, and waveform.

Protection

The output of these V to F's may be shorted to common indefinitely, and to $+V_{cc}$ for several microseconds, but they must *never* be connected to $-V_{cc}$ or failure will result.

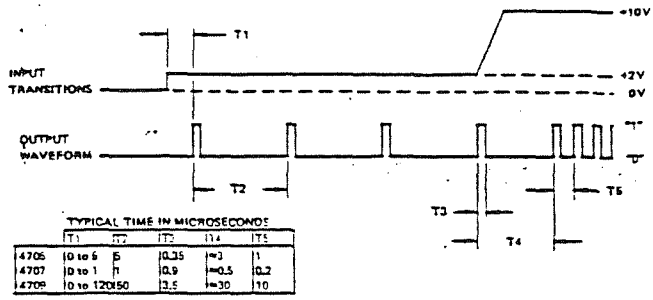
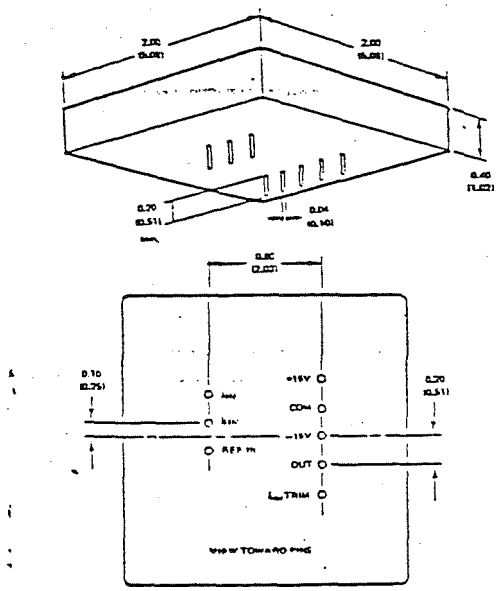


Figure 7. V to F Output Waveform & Timing



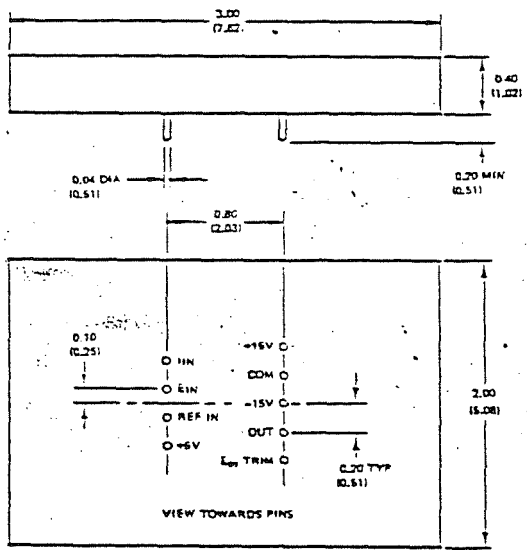
Mechanical Dimensions for 4705 & 4709

4705/4707/4709

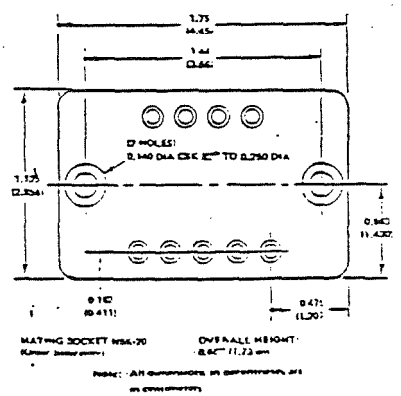
SPECIFICATIONS @25 °C, V_{cc} = ±15 V (unless otherwise indicated)

	4709		4705		4707	
	TYPICAL	GUARANTEED	TYPICAL	GUARANTEED	TYPICAL	GUARANTEED
FULL SCALE FREQUENCY (FS f_{out})	100 kHz		1 MHz		5 MHz	
ANALOG INPUT						
Signal Range, relative to ±V_{cc} Common						
@ +V_{in}	10 µV to 12 V	100 µV to 11 V	10 µV to 12 V	100 µV to 10.5 V	10 µV to 12 V	100 µV to 10.5 V
@ +I_{in} (±25%)	—	450 pA to 450 µA	—	850 pA to 850 µA	—	900 pA to 900 µA
@ −V_{in}	10 µV to 100 mV	—	10 µV to 1 V	—	10 µV to 1 V	—
Common Mode Voltage Range (see Fig. 6D)	±100 mV	—	±1 V	—	±1 V	—
Common Mode Rejection Ratio (at CMV)	60 dB	—	60 dB	—	60 dB	—
Offset Voltage (trimmable to zero)	±1 mV	±3 mV	±3 mV	±10 mV	±3 mV	±10 mV
Impedance @ +V_{in} (±25%)	—	23 KΩ	—	11 KΩ	—	12 KΩ
Overvoltage Protection @ +V_{in} and −V_{in}	±V_{cc}	—	±V_{cc}	—	±V_{cc}	—
Overcurrent Protection @ +I_{in}	150% max. I_{in}	—	150% max. I_{in}	—	150% max. I_{in}	—
FREQUENCY OUTPUT — NONLINEARITY						
Ideal Transfer Function over Signal Range @ +V_{in}	(100 kHz)(V_{in}/10 V)		(1 MHz)(V_{in}/10 V)		(5 MHz)(V_{in}/10 V)	
Nonlinearity, ±% Full Scale plus ± %Signal	100 µV to 11 V		100 µV to 10.5 V		200 µV to 10.5 V	
@ 25 °C	0.001 ± 0.004	0.005 ± 0.02	0.0002 ± 0.012	0.001 ± 0.05	0.004 ± 0.02	0.01 + 0.05
From 0 °C to +70 °C (4709)	0.001 ± 0.006	0.01 ± 0.03				
From 0 °C to +50 °C (4705/4707)			0.0003 ± 0.03	—	0.005 ± 0.03	0.02 + 0.08
@ 25 °C (4705-01)				0.0005 ± 0.02		
Full Scale Factor (V_{in} for FS f_{out}, trimmable to 10 V)	—	9.9 ± 0.05	—	9.9 ± 0.05	—	9.9 ± 0.05
Wave Form/Timing (See Fig. 7) ①						
Pulse Characteristics						
"1" (HIGH) No Load/+0.4 mA Load	—	+5V±0.5V/+2.4 V	—	+5V±0.5V/+2.4 V	—	+5V±0.5V/+2.4 V
"0" (LOW)	—	+0.2V±0.2V @ −16mA sink current	—	+0.2V±0.2V @ −16mA sink current	—	+0.2V±0.2V @ −16mA sink current
Width	3.5 µsec	2.5 µs to 4.5 µs	0.35 µsec	0.2 µsec to 0.5 µsec	90 nsec	50 nsec to 150 nsec
Output Impedance (High State) ±20%	—	3 KΩ	—	680 Ω	—	680 Ω
Fan Out	—	10 TTL Loads	—	10 TTL Loads	—	10 TTL Loads
RESPONSE						
Settling Time to 0.01% for Step Input (typical)	1 to 2 pulses of new freq. +10 µsec	—	1 to 2 pulses of new freq. +10 µsec	—	1 to 2 pulses of new freq. +10 µsec	—
Overload Recovery	20 msec	—	1 msec	—	5 µsec	—
Allowable Capacitive Load for Rated Performance	500 pF	—	100 pF	—	50 pF	—
STABILITY OF FULL SCALE FREQUENCY						
Temperature Coefficient ±PPM/°C						
4709/4705/4705-01/4707	—	44	44	200	80	150
4709-02	—	12				
Power Supply Sensitivity, ±PPM/%ΔV_{cc}	—	100	—	500	—	1500
Drift Per Day/Per Month ±PPM	10/30	—	100/200	—	150/300	—
STABILITY OF ZERO OFFSET VOLTAGE						
Temperature Coefficient ±µV/°C	3	30	10	50	30	100
Power Supply Sensitivity ±µV/%ΔV_{cc} (V trim constant)	—	50	—	100	—	300
Warm Up Time to 0.1%	< 10 min.	—	< 10 min.	—	< 10 min.	—
POWER REQUIREMENT						
Voltage Range ±V_{cc}	±12 V to ±18 V	±15 V ±1%	±12 V to ±18 V	±15 V ±5%	—	±15V±1%, ±0.1% reg.
Auxiliary	—	—	—	—	—	+5 V ±5%, ±0.5% reg.
Current: ±I_{cc} @ ±V_{cc} = ±15 V	—	±18 mA	—	±24 mA	—	−40 mA, −20 mA
Auxiliary @ +5 V	—	—	—	—	—	+50 mA
ENVIRONMENT/RELIABILITY						
Operating Temperature Range	−25 to +85 °C	0 to +70 °C	−25 to +85 °C	0 to +70 °C	−25 to +85 °C	0 to +70 °C
Storage Temperature Range	—	−55 to +125 °C	—	−55 to +125 °C	—	−55 to +125 °C
Warning!! Do not connect output pin to −V_{cc} or device will fail!! Output may be connected to common momentarily, and to +V_{cc} for 5 seconds.						
Suggested Philbrick Power Supplies	2209, 2403, 2301		2209, 2403, 2301		2242, 2231	

① Train of TTL compatible pulses at f_{out} pin adaptable to CMOS and HNIL



Mechanical Dimensions for 4707



Recommended Socket: NSK-20

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